
YAMAHA[®] LSI

YMF715

OPL3-SA3

OPL3 Single-chip Audio System 3

■ OUTLINE

YMF715-S (OPL3-SA3) is a single audio chip that integrates OPL3 and its DAC, 16bit Sigma-delta CODEC, MPU401 MIDI interface, joystick port, and a 3D enhanced controller including all the analog components which is suitable for multi-media application. This LSI is fully compliant with Plug and Play ISA 1.0a, and supports all the necessary features, i.e. 16bit address decode, more IRQs and DMAs in compliance with PC'96. This LSI also supports the expandability, i.e. Zoomed Video, Modem and CD-ROM interface in a Plug and Play manner, and power management(power down, power save, partial power down, and suspend/resume) that is indispensable with power-conscious application.

■ FEATURES

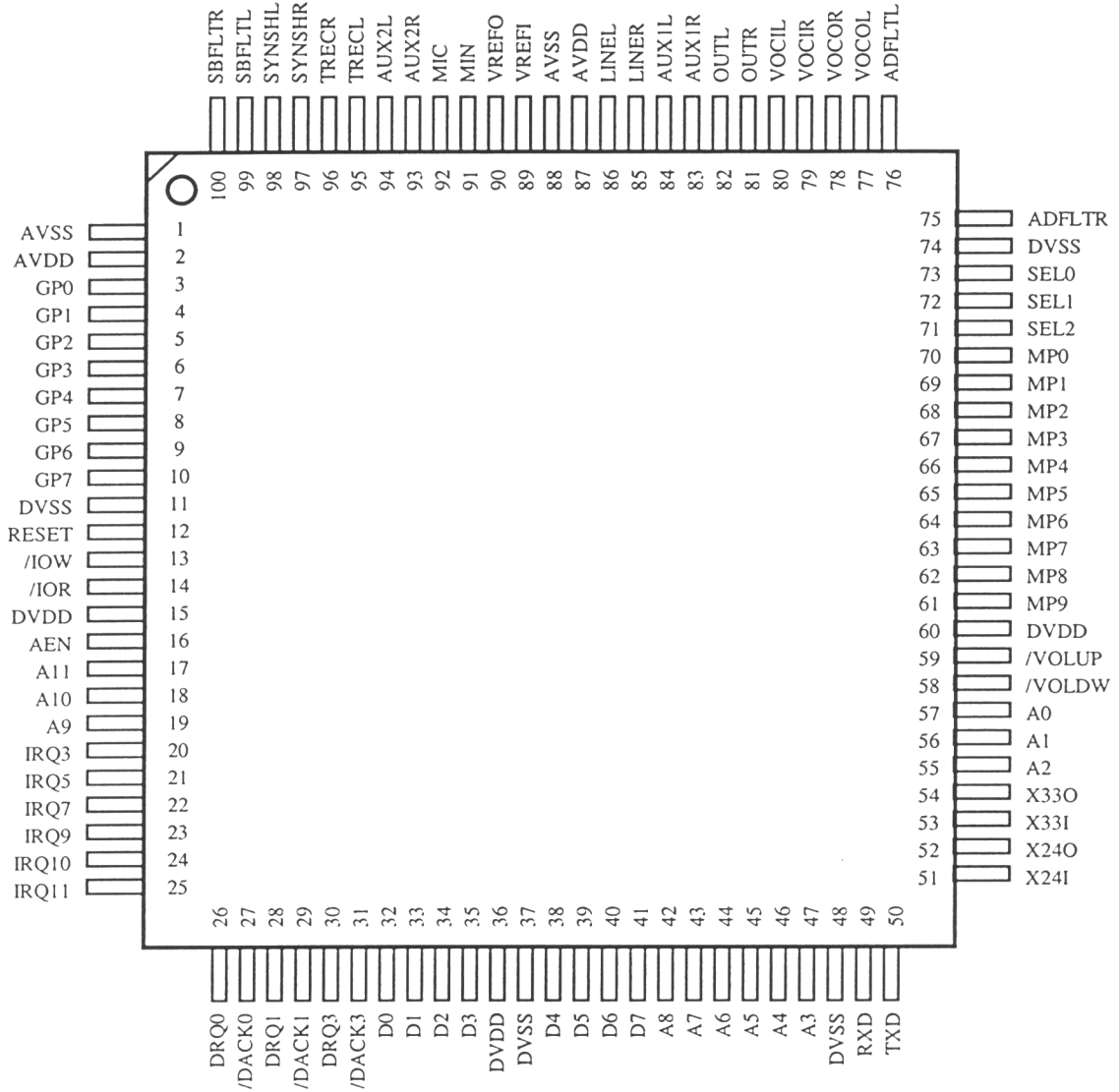
- Built-in OPL3 (FM-synthesizer)
- Supports Sound Blaster Game compatibility
- Supports Windows Sound System compatibility
- Supports Plug & Play ISA 1.0a compatibility
- Full Duplex operation
- Built-in MPU401 Compatible MIDI I/O port
- Built-in Joystick port
- Built-in the 3D enhanced controller including all the analog components
- Supports multi-purpose pin function
(Support 16-bit address decode, DAC interface for OPL4-ML, Zoomed Video port, EEPROM interface, MODEM interface, IDE CD-ROM interface)
- Hardware and software master volume control
- Supports monaural input
- 24 mA TTL bus drive capability
- Supports Power Management(power down, power save, partial power down, and suspend/resume)
- +5V/ +3.3V power supply for digital, 5V power supply for analog.
- 100 pin SQFP package (YMF715-S)

YAMAHA CORPORATION

February 21, 1997

■ PIN CONFIGURATION

YMF715-S



100 pin SQFP Top View

■ PIN DESCRIPTION

ISA bus interface: 36 pins					
name	pins	I/O	type	Size	function
D7-0	8	I/O	TTL	24mA	Data Bus
A11-0	12	I	TTL	-	Address Bus
AEN	1	I	TTL	-	Address Bus Enable
/IOW	1	I	Schmitt	-	Write Enable
/IOR	1	I	Schmitt	-	Read Enable
RESET	1	I	Schmitt	-	Reset
IRQ3,5,7,9,10,11	6	T	TTL	12mA	Interrupt request
DRQ0, 1, 3	3	T	TTL	12mA	DMA Request
/DACK0, 1, 3	3	I	TTL	-	DMA Acknowledge

Analog Input & Output : 24 pins					
name	pins	I/O	type	size	function
OUTL	1	O	-	-	Left mixed analog output
OUTR	1	O	-	-	Right mixed analog output
VREFI	1	I	-	-	Voltage reference input
VREFO	1	O	-	-	Voltage reference output
AUX1L	1	I	-	-	Left AUX1 input
AUX1R	1	I	-	-	Right AUX1 input
AUX2L	1	I	-	-	Left AUX2 input
AUX2R	1	I	-	-	Right AUX2 input
LINEL	1	I	-	-	Left LINE input
LINER	1	I	-	-	Right LINE input
MIC	1	I	-	-	MIC input
MIN	1	I	-	-	Monaural input
TRECL	1	-	-	-	Left Treble capacitor
TRECR	1	-	-	-	Right Treble capacitor
SBFLTL	1	-	-	-	Left SBDAC filter
SBFLTR	1	-	-	-	Right SBDAC filter
SYNSHL	1	-	-	-	Left SYNDAC sample / hold capacitor
SYNSHR	1	-	-	-	Right SYNDAC sample / hold capacitor
ADFLTL	1	-	-	-	Left input filter
ADFLTR	1	-	-	-	Right input filter
VOCOL	1	O	-	-	Left voice output
VOCOR	1	O	-	-	Right voice output
VOCIL	1	I	-	-	Left voice input
VOCIR	1	I	-	-	Right voice input

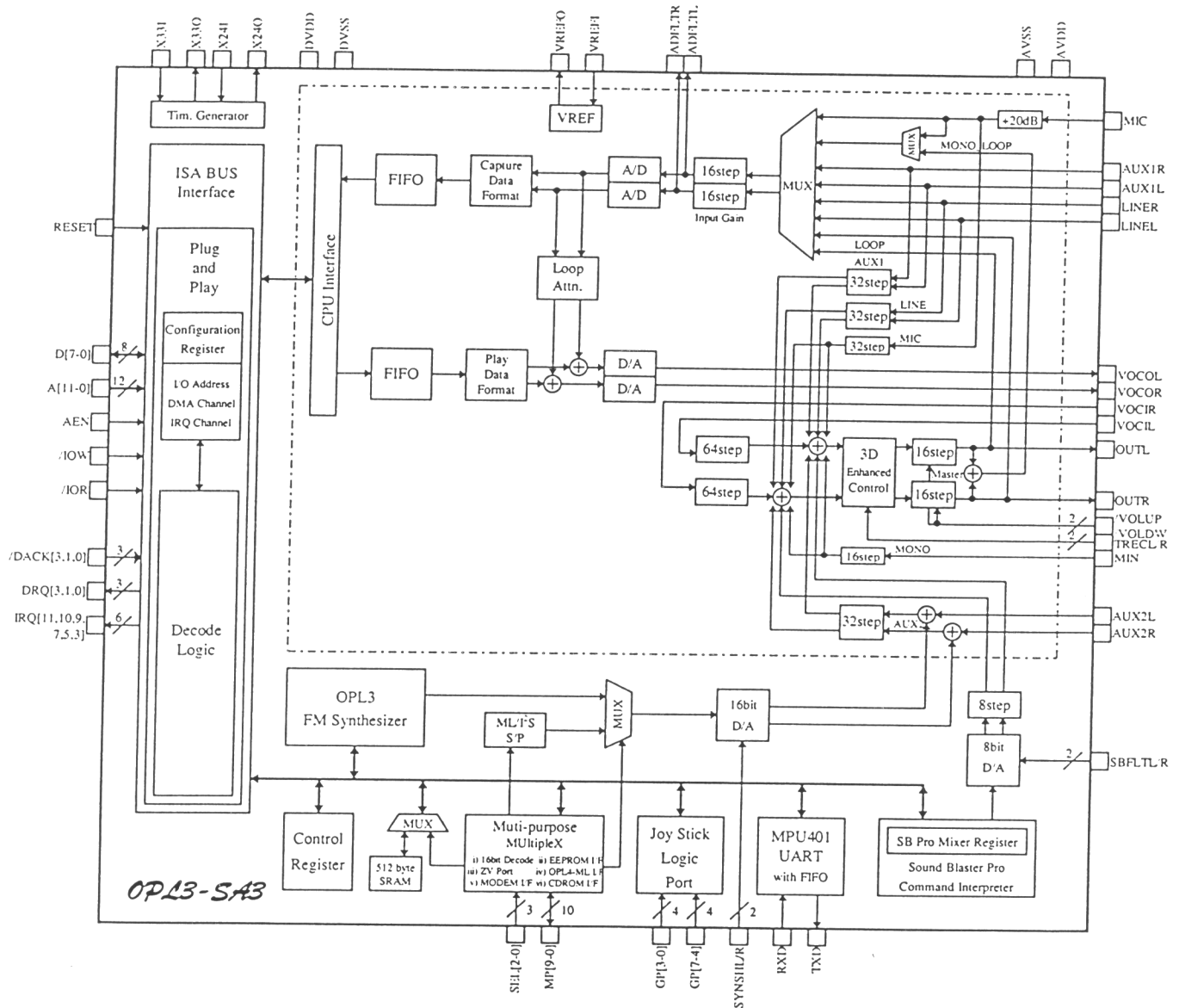
Multi-purpose pins : 13 pins					
name	pins	I/O	type	size	function
SEL2-0	3	I+	CMOS	-	Refer to "Multi-purpose pins" section
MP9-0	10	I+/O	TTL	2mA	Refer to "multi-purpose pins" section

Others : 27 pins					
name	pins	I/O	type	size	function
GP3-0	4	IA	-	-	Game Port
GP7-4	4	I+	Schmitt	-	Game Port
RXD	1	I+	Schmitt	-	MIDI Data Receive
TXD	1	O	TTL	4mA	MIDI Data Transfer
/VOLUP	1	I+	Schmitt	-	Hardware Volume (Up)
/VOLDW	1	I+	Schmitt	-	Hardware Volume (Down)
X33I	1	I	CMOS	-	33.8688 MHz
X33O	1	O	CMOS	2mA	33.8688 MHz
X24I	1	I	CMOS	-	24.576 MHz
X24O	1	O	CMOS	2mA	24.576 MHz
AVDD	2	-	-	-	Analog Power Supply (put on +5.0V)
DVDD	3	-	-	-	Digital Power Supply (put on +5.0 V or +3.3V)
AVSS	2	-	-	-	Analog GND
DVSS	4	-	-	-	Digital GND

Total : 100 pins

Note: I+: Input Pin with Pull up Resistor T: TTL-tri-state output pin
 Schmitt: TTL-Schmitt input pin

■ BLOCK DIAGRAM



■ FUNCTION OVERVIEW

1. Multi-purpose pin

1-1. Multi-purpose function

OPL3-SA3 can support the various functions listed below by programming SEL2-0 pins.

- A. 16-bit address decode
- B. EEPROM interface
- C. Zoomed video port
- D. CPU and DAC interface for OPL4-ML
- E. MODEM interface
- F. IDE CD-ROM interface

Following table shows what combinations of the above functions are available for each SEL2-0 pins.

SEL	16bit Dec.	EEPROM	ZV port	OPL4-ML	MODEM	CDROM	Remark
0	-	-	-	-	-	-	Test mode
1	○(*1)	○	-	○(*2)	○	○(*1)	S/C,C/C(add-in)
2	○	○	-	○(*3)	○	-	S/C (add-in)
3	○(*4)	○	-	○	-	-	S/C (add-in)
4	○(*4)	-	○	○	-	-	Note PC
5	○	-	○	○(*3)	○	-	Note PC
6	-	-	-	-	-	-	reserved
7	○	-	-	○	-	-	M/B, Note PC

Where,

S/C : Sound Card

C/C : Combo Card (Sound and Modem)

M/B : Desktop Mother Board

	SEL=0	SEL=1	SEL=2	SEL=3	SEL=4	SEL=5	SEL=6	SEL=7
SEL0 pin	0	1	0	1	0	1	0	1
SEL1 pin	0	0	1	1	0	0	1	1
SEL2 pin	0	0	0	0	1	1	1	1

Notice

*1 : External PAL is needed.

*2 : External wavetable synthesizer (ex.OPL4-ML) is mixed as analog signal using external DAC.

*3 : Clock module (ex.MK1420) is used to generate the clock for OPL4-ML and it will be mixed analog signal by having an additional DAC.

*4 : External TTLs (ex.LS138) is needed.

See section 1-2 and 1-3 for implementation detail.

1-2. Pin description

	SEL=0	SEL=1	SEL=2	SEL=3	SEL=4	SEL=5	SEL=6	SEL=7
MP0	-	/MCS	/MCS	/EXTEN	/EXTEN	/MCS	-	/EXTEN
MP1	-	MIRQ	MIRQ	/SYNCS	/SYNCS	MIRQ	-	/SYNCS
MP2	-	ROMCLK	ROMCLK	ROMCLK	BCLK_ZV	A12	-	A12
MP3	-	ROMCS	ROMCS	ROMCS	LRCK_ZV	A13	-	A13
MP4	-	ROMDI	ROMDI	ROMDI	SIN_ZV	A14	-	A14
MP5	-	ROMDO	ROMDO	ROMDO	/XRST	A15	-	A15
MP6	-	/CDCS0	A12	BCLK_ML	BCLK_ML	BCLK_ZV	-	BCLK_ML
MP7	-	/CDCS1	A13	LRCK_ML	LRCK_ML	LRCK_ZV	-	LRCK_ML
MP8	-	CDIRQ	A14	SIN_ML	SIN_ML	SIN_ZV	-	SIN_ML
MP9	-	CLKO	A15	CLKO	CLKO	/XRST	-	CLKO

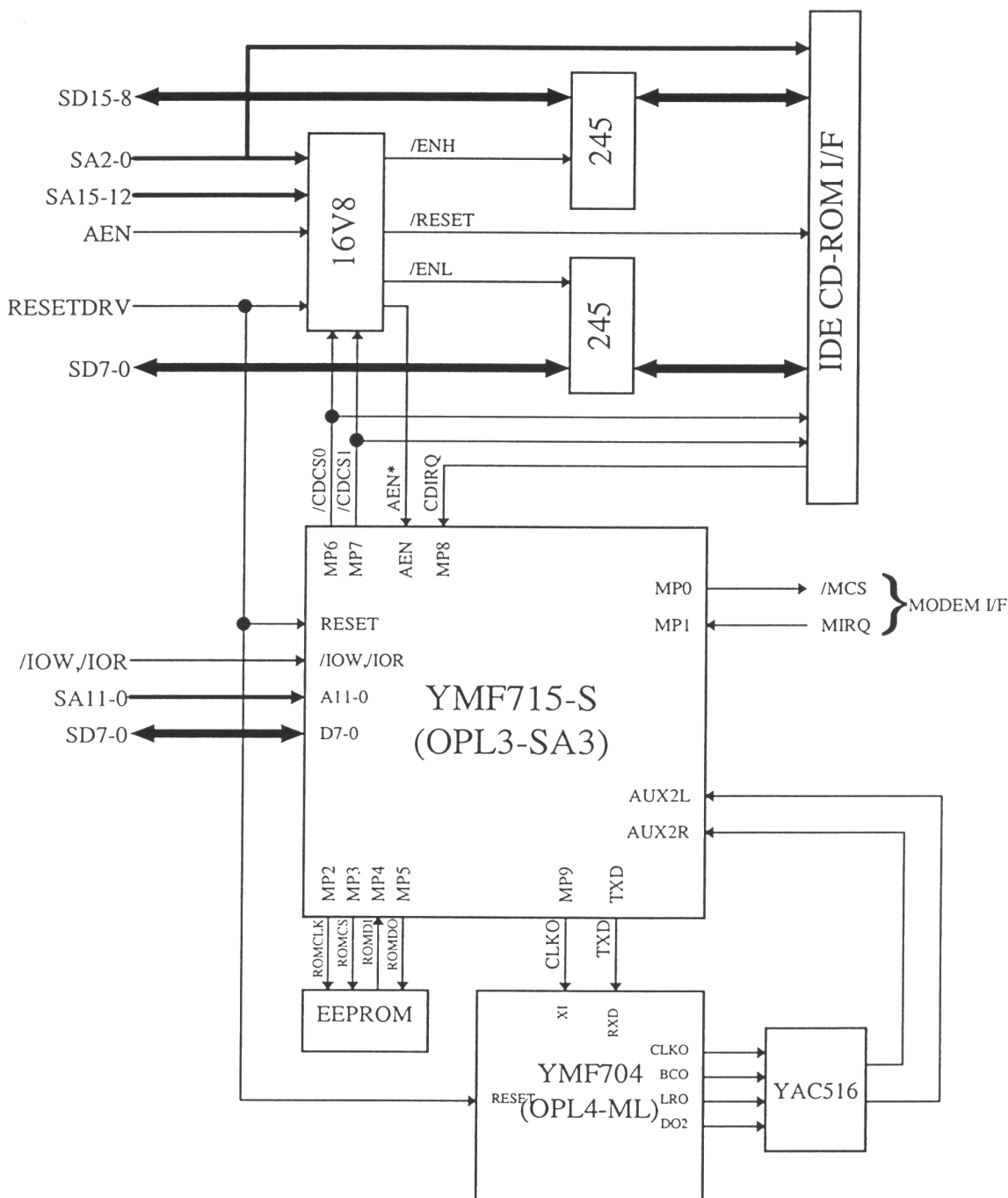
Note: do not select SEL=0 and SEL=6.

SEL=0;TEST mode SEL=6;reserved

Mutil-purpose pins:		
name	I/O	function
/MCS	O	Chip select output for MODEM chip (COM)
MIRQ	I+	Interrupt request input for MODEM (COM)
ROMCLK	O	Serial data clock output for external EEPROM
ROMCS	O	Chip select output for external EEPROM
ROMDI	I+	Serial data input for external EEPROM
ROMDO	O	Serial data output for external EEPROM
/CDCS0	O	Chip select output for IDE CD-ROM (/CS1FX)
/CDCS1	O	Chip select output for IDE CD-ROM (/CS3FX)
CDIRQ	I+	Interrupt request input for IDE CD-ROM
A12 - 15	I	Address bus for ISA-bus
/EXTEN	I+	Enable OPL4-ML interface
/SYNCS	O	Chip select output for OPL4-ML
BCLK_ML	I+	Bit clock input for OPL4-ML
LRCK_ML	I+	L/R clock input for OPL4-ML
SIN_ML	I+	Serial data input for OPL4-ML
CLKO	O	Master clock output (33.8688MHz)
BCLK_ZV	I+	Bit clock input for Zoomed Video port (I ² S)
LRCK_ZV	I+	L/R clock input for Zoomed Video port (I ² S)
SIN_ZV	I+	Serial data input for Zoomed Video port (I ² S)
/XRST	O	Inverted RESET output

1-3. System Block Diagram

(1) SEL=1 (Sound Card and Combo Card Add-in)



1. External PAL(16V8 etc.)

- (i) connect the signal AEN* generated by decoding SA15-12 and AEN to the AEN of OPL3-SA3.
- (ii) generate the /G(enable) signal for Data Bus Buffer (LS245) by decoding the /CDCS1-0 and SA2-0.
- (iii) generate the /RESET signal from RESETDRV.

1-2. Pin description

	SEL=0	SEL=1	SEL=2	SEL=3	SEL=4	SEL=5	SEL=6	SEL=7
MP0	-	/MCS	/MCS	/EXTEN	/EXTEN	/MCS	-	/EXTEN
MP1	-	MIRQ	MIRQ	/SYNCS	/SYNCS	MIRQ	-	/SYNCS
MP2	-	ROMCLK	ROMCLK	ROMCLK	BCLK_ZV	A12	-	A12
MP3	-	ROMCS	ROMCS	ROMCS	LRCK_ZV	A13	-	A13
MP4	-	ROMDI	ROMDI	ROMDI	SIN_ZV	A14	-	A14
MP5	-	ROMDO	ROMDO	ROMDO	/XRST	A15	-	A15
MP6	-	/CDCS0	A12	BCLK_ML	BCLK_ML	BCLK_ZV	-	BCLK_ML
MP7	-	/CDCS1	A13	LRCK_ML	LRCK_ML	LRCK_ZV	-	LRCK_ML
MP8	-	CDIRQ	A14	SIN_ML	SIN_ML	SIN_ZV	-	SIN_ML
MP9	-	CLKO	A15	CLKO	CLKO	/XRST	-	CLKO

Note: do not select SEL=0 and SEL=6.

SEL=0;TEST mode SEL=6;reserved

Mutil-purpose pins:		
name	I/O	function
/MCS	O	Chip select output for MODEM chip (COM)
MIRQ	I+	Interrupt request input for MODEM (COM)
ROMCLK	O	Serial data clock output for external EEPROM
ROMCS	O	Chip select output for external EEPROM
ROMDI	I+	Serial data input for external EEPROM
ROMDO	O	Serial data output for external EEPROM
/CDCS0	O	Chip select output for IDE CD-ROM (/CS1FX)
/CDCS1	O	Chip select output for IDE CD-ROM (/CS3FX)
CDIRQ	I+	Interrupt request input for IDE CD-ROM
A12 - 15	I	Address bus for ISA-bus
/EXTEN	I+	Enable OPL4-ML interface
/SYNCS	O	Chip select output for OPL4-ML
BCLK_ML	I+	Bit clock input for OPL4-ML
LRCK_ML	I+	L/R clock input for OPL4-ML
SIN_ML	I+	Serial data input for OPL4-ML
CLKO	O	Master clock output (33.8688MHz)
BCLK_ZV	I+	Bit clock input for Zoomed Video port (I ² S)
LRCK_ZV	I+	L/R clock input for Zoomed Video port (I ² S)
SIN_ZV	I+	Serial data input for Zoomed Video port (I ² S)
/XRST	O	Inverted RESET output

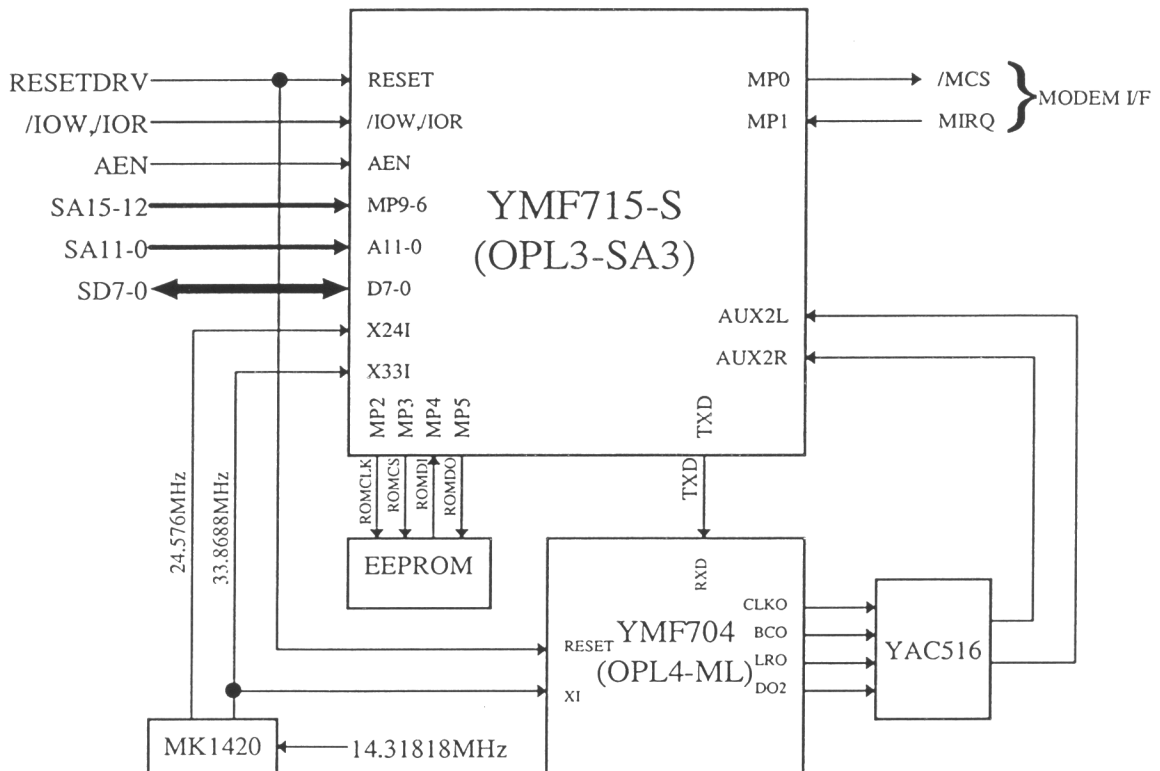
2. Master Clock

Both 33.8688MHz and 24.576MHz are used or 14.31818MHz and clock module (ex.MK1420 by Micro Clock) are used.

3. YMF704(OPL4-ML)

The external DAC (YAC516) is necessary for wavetable upgrade.

(2) SEL=2 (Sound Card and Combo Card for Add-in)



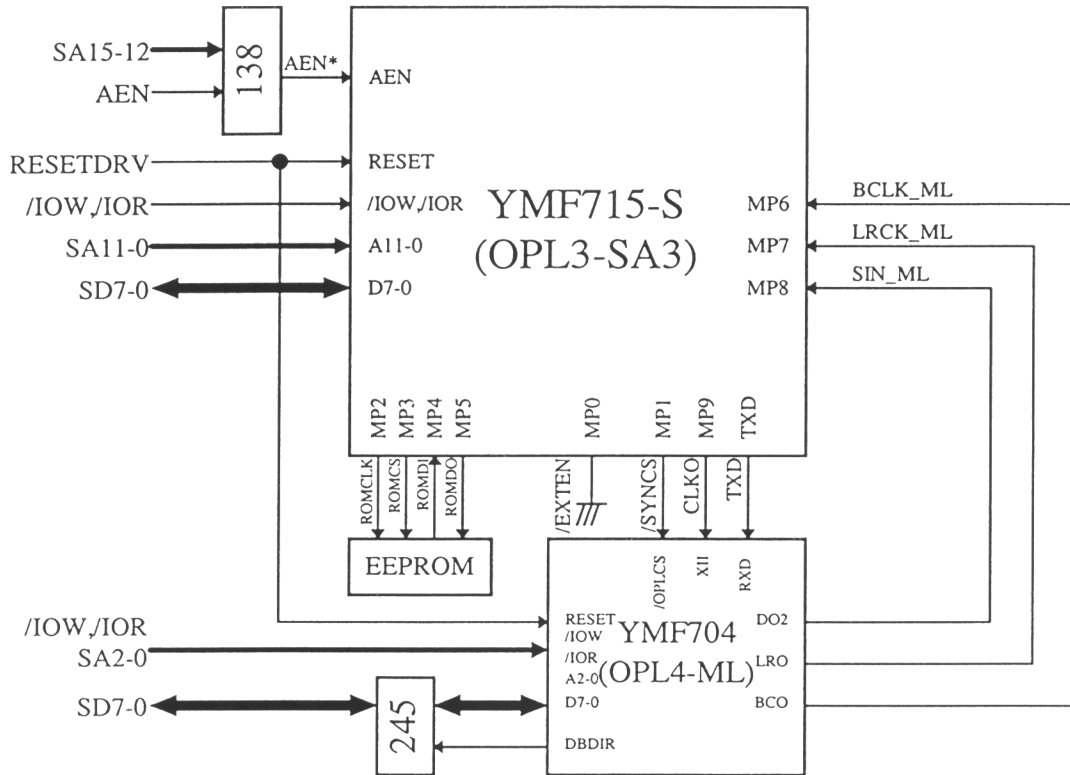
1. YMF704(OPL4-ML)

The external DAC (YAC516) and the clock module (ex.MK1420 by Micro Clock) are necessary for wavetable upgrade.

2. MK1420

The MK1420 is the clock module that generates all clocks necessary for this chipset . It is by Micro Clock and its package is SOP8.

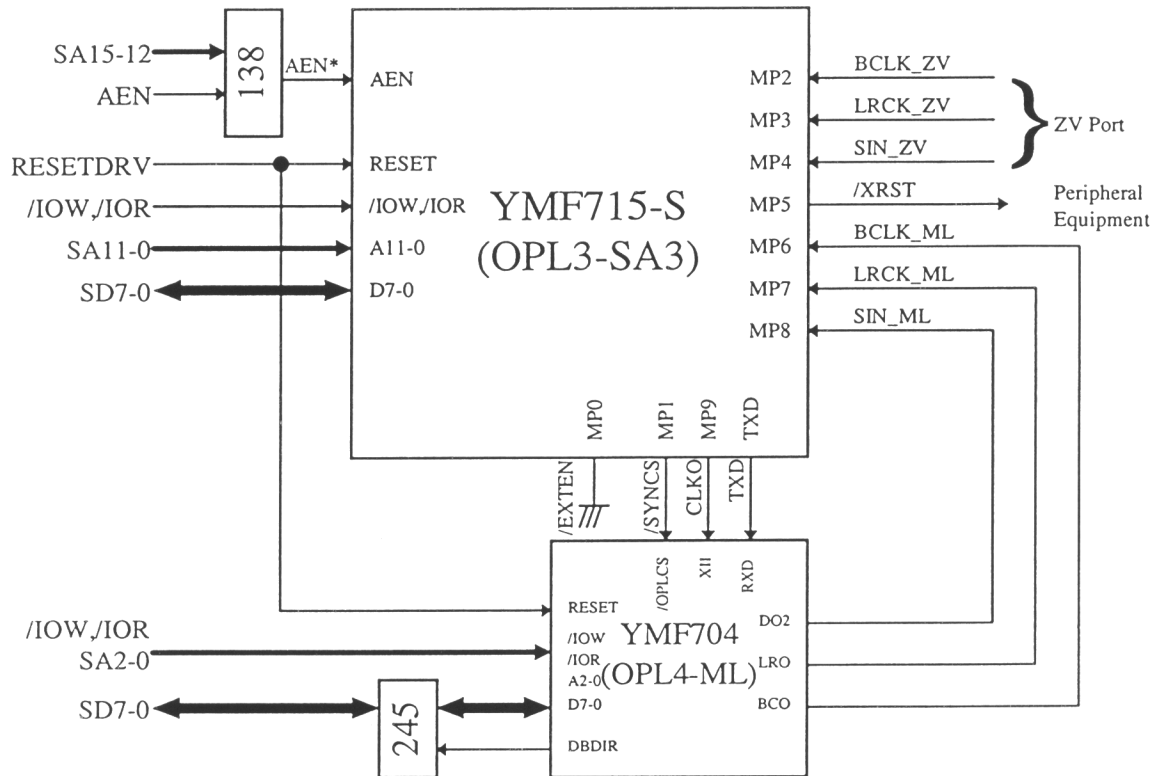
(3) SEL=3 (Sound Card for Add-in)



1.16bit Address Decode

The signal AEN* generated by decoding SA15-12 and AEN needs to be connected to the AEN of OPL3-SA3.

(4) SEL=4 (for Notebook PC)



1. 16bit Address Decode

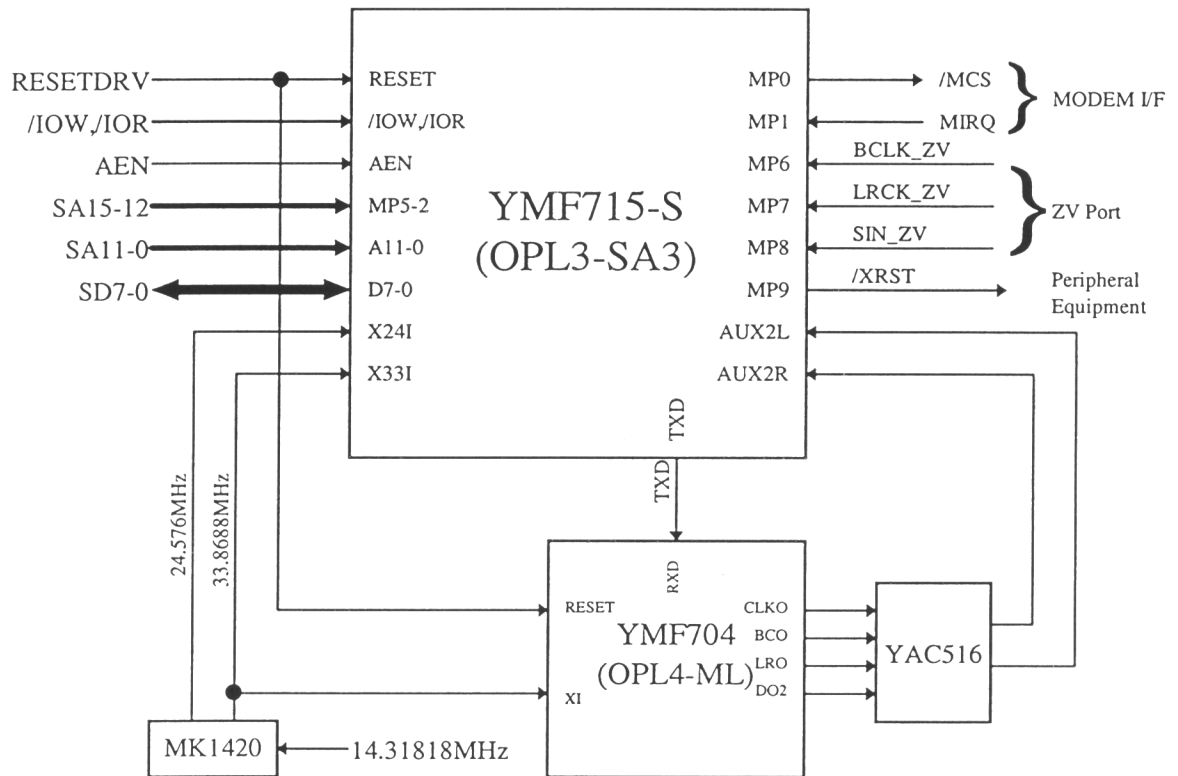
The signal AEN* generated by decoding SA15-12 and AEN needs to be connected to the AEN of OPL3-SA3.

2. ZV Port and YMF704(OPL4-ML) I/F

ZV port is supported by using the internal DAC of OPL3-SA3 that is originally dedicated for the use of internal OPL3.

- (i) either OPL4-ML or ZV port is active at a time and simultaneous use is not possible.
- (ii) which function the internal DAC is used for is determined by the SA3 Control register, index 02h, VZE bit.

(5) SEL=5 (for Notebook PC)



1. Internal DAC

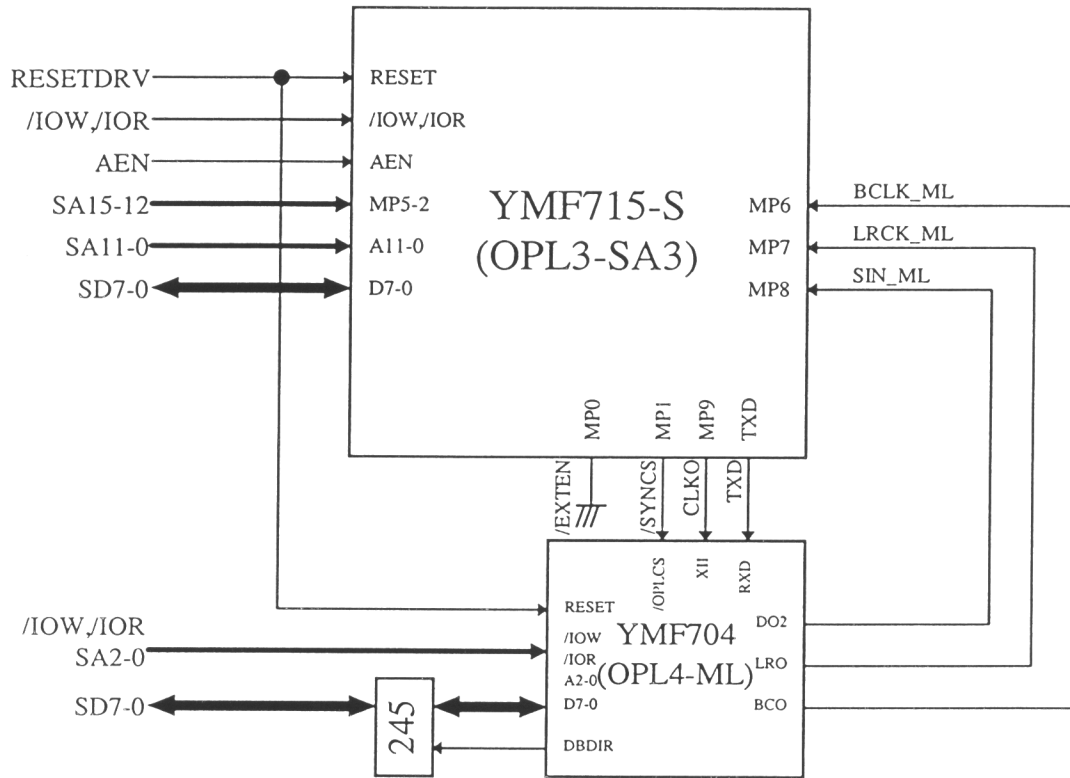
The internal OPL3 and the ZV Port shares the internal DAC, which is very similar to the case mentioned the previous section.

- (i) either internal OPL3 or ZV port is active at a time and simultaneous use is not possible.
- (ii) which function the internal DAC is used for is determined by the SA3 control register, index 02h, VZE bit.

2. YMF704(OPL4-ML)

The external DAC (YAC516) and the clock module (ex.MK1420 by Micro Clock) are necessary for wave table upgrade.

(6) SEL=7 (for Notebook PC, Desktop PC)



2. ISA Interface

OPL3-SA3 supports ISA Plug and Play (PnP) that frees the users from configuring the I/O address, IRQ and DMA channel. Those system resources are set automatically by the system. However even when used in Non PnP system, the configuration can be changed with software.

2-1. PnP Auto-Configuration mode

OPL3-SA3 has the following I/O port to support the Plug and Play ISA.

Address port:	279h
Write Data Port:	A79h
Relocatable Read Data Port:	203h - 03FFh

The following four Logical Devices are supported by OPL3-SA3.

Logical Device No. 0

Sound Blaster compatible Playback system	(SB Base)
16-bit CODEC	(WSS Base)
MPU401	(MPU Base)
OPL3	(AdLib Base)
OPL3-SA3 control register	(CTRL Base)

Logical Device No. 1

Joy Stick

Logical Device No. 2 (Optional)

MODEM (COM port)

Logical Device No. 3 (Optional)

IDE CD-ROM interface

TAL

Logical Device Number = 0 : SA3 Sound System

30h	R/W	Activate
60h	R/W	I/O port base address[15..8], Descriptor 0 (SB base)
61h	R/W	I/O port base address[7..0], Descriptor 0 (SB base)
62h	R/W	I/O port base address[15..8], Descriptor 1 (WSS base)
63h	R/W	I/O port base address[7..0], Descriptor 1 (WSS base)
64h	R/W	I/O port base address[15..8], Descriptor 2 (AdLib base)
65h	R/W	I/O port base address[7..0], Descriptor 2 (AdLib base)
66h	R/W	I/O port base address[15..8], Descriptor 3 (MPU base)
67h	R/W	I/O port base address[7..0], Descriptor 3 (MPU base)
68h	R/W	I/O port base address[15..8], Descriptor 4 (CTRL base)
69h	R/W	I/O port base address[7..0], Descriptor 4 (CTRL base)
70h	R/W	Interrupt request level select 0 (for IRQ-A)
71h	R	Interrupt request type select 0 (for IRQ-A)
72h	R/W	Interrupt request level select 1 (for IRQ-B)
73h	R	Interrupt request type select 1 (for IRQ-B)
74h	R/W	DMA channel select 0 (for DMA-A)
75h	R/W	DMA channel select 1 (for DMA-B)

Logical Device Number = 1 : Joystick

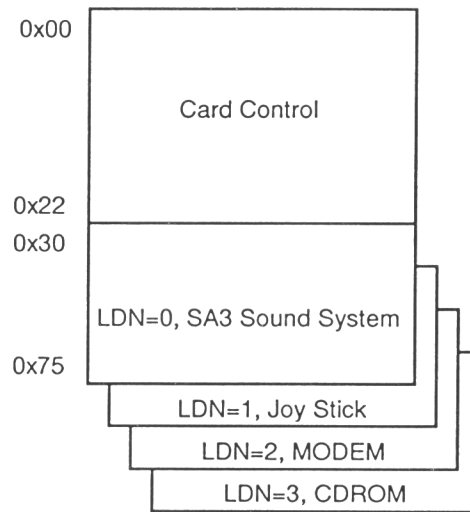
30h	R/W	Activate
60h	R/W	I/O port base address[15..8]
61h	R/W	I/O port base address[7..0]

Logical Device Number = 2 : MODEM (Optional)

30h	R/W	Activate
60h	R/W	I/O port base address[15..8]
61h	R/W	I/O port base address[7..0]
70h	R/W	Interrupt request level select
71h	R	Interrupt request type select

2-2. PnP ISA Configuration Register

OPL3-SA3 has the following Registers defined in the PnP ISA software.



Listed below is the register map of card control register and logical device registers. For the detailed description of each register, please refer to the *Plug and Play ISA Specification 1.0a*

Card Control Registers

Index	R/W	D7	D6	D5	D4	D3	D2	D1	D0	
00h	W	Set RD_DATA								
01h	R	Serial Isolation								
02h	W	Config Control								
03h	W	Wake [CSN]								
04h	R	Resource Data								
05h	R	Status								
06h	R/W	Card Select Number								
07h	R/W	Logical Device Number								
20h	W	Resource Data Write								
21h	W								IKD	RDWE

Note:

RDWE : Resource Data Write Enable

Setting to "1" this bit means the host can download the resources data to EEPROM and internal SRAM via 20h.

IKD : Initiation Key Disable

Setting to "1" this bit means OPL3-SA3 should not detect the initiation key in the Wait for Key state.

Logical Device Number = 3 : CD-ROM (Optional)

30h	R/W	Activate
60h	R/W	I/O port base address [15..8], Descriptor 0 (/CDCS0)
61h	R/W	I/O port base address [7..0], Descriptor 0 (/CDCS0)
62h	R/W	I/O port base address [15..8], Descriptor 1 (/CDCS1)
63h	R/W	I/O port base address [7..0], Descriptor 1 (/CDCS1)
70h	R/W	Interrupt request level select
71h	R	Interrupt request type select

2-3. Recommended Resource Data

The recommended resource data is the followings.

(1) LDN=0:SA3 Sound System

I/O (SB base): 16bit address decode

Index	Best	Acceptable1	Acceptable2	Acceptable3
I/O	220h	240h	220-280h	<-
Length	16	16	16	<-
Alignment	-	-	16	<-

I/O (WSS base): 16bit address decode

Index	Best	Acceptable1	Acceptable2	Acceptable3
I/O	530h	E80h	530-F48h	<-
Length	8	8	8	<-
Alignment	-	-	8	<-

I/O (AdLib base): 16bit address decode

Index	Best	Acceptable1	Acceptable2	Acceptable3
I/O	388h	<-	388-3F8h	<-
Length	8	<-	8	<-
Alignment	-	-	8	<-

I/O (MPU base): 16bit address decode

Index	Best	Acceptable1	Acceptable2	Acceptable3
I/O	330h	300h	300-334h	<-
Length	2	2	2	<-
Alignment	-	-	2	<-

I/O (CTRL base): 16bit address decode

Index	Best	Acceptable1	Acceptable2	Acceptable3
I/O	370h	100-FFEh	<-	<-
Length	2	2	<-	<-
Alignment	-	2	<-	<-

IRQ-A: high-active, edge-sense

Index	Best	Acceptable1	Acceptable2	Acceptable3
IRQ	10	5,7,9,10,11	3,5,7,9,10,11	<-

IRQ-B: high-active, edge-sense

Index	Best	Acceptable1	Acceptable2	Acceptable3
IRQ	5	5,7,9,10,11	3,5,7,9,10,11	<-

DMA-A:8bit, count by byte, type-A, B, F

Index	Best	Acceptable1	Acceptable2	Acceptable3
DMA	0	0,1,3	0,1,3	<-

DMA-B:8bit, count by byte, type-A, B, F

Index	Best	Acceptable1	Acceptable2	Acceptable3
DMA	1	0,1,3	0,1,3	<-

(2) LDN=1:Joystick

I/O (Game Port): 16bit address decode

Index	Best	Acceptable1	Acceptable2	Acceptable3
I/O	201h	202h	203h	204-20Fh
Length	1	1	1	1
Alignment	-	-	-	1

(3) LDN=2:MODEM

I/O (/MCS): 16bit address decode

Index	Best	Acceptable1	Acceptable2	Acceptable3
I/O	2F8h	100-FF8h	<-	<-
Length	8	8	<-	<-
Alignment	-	8	-	-

IRQ: high-active, edge-sense

Index	Best	Acceptable1	Acceptable2	Acceptable3
IRQ	3	<-	<-	<-

(4) LDN=3:CD-ROM

I/O (/CDCS0): 16bit address decode

Index	Best	Acceptable1	Acceptable2	Acceptable3
I/O	1E8h	100-1F8h	<-	<-
Length	8	8	<-	<-
Alignment	-	8	<-	<-

I/O (/CDCS1): 16bit address decode

Index	Best	Acceptable1	Acceptable2	Acceptable3
I/O	3EEh	306-3F6h	<-	<-
Length	1	1	<-	<-
Alignment	-	8	<-	<-

IRQ: high-active, edge-sense

Index	Best	Acceptable1	Acceptable2	Acceptable3
IRQ	11	3,5,7,9,10,11	<-	<-

2-4. Manual Configuration Mode

When OPL3-SA3 is in the Wait for Key state, it can be changed to the Manual Configuration mode by sending the following YAMAHA key to Address_Port. The Manual Configuration mode is used for downloading the resource data to EEPROM and internal SRAM, setting up the OPL3-SA3 without PnP protocol.

YAMAHA Key:

B1h, D8h, 6Ch, 36h, 9Bh, 4Dh, A6h, D3h,
69h, B4h, 5Ah, ADh, D6h, EBh, 75h, BAh,
DDh, EEh, F7h, 7Bh, 3Dh, 9Eh, CFh, 67h,
33h, 19h, 8Ch, 46h, A3h, 51h, A8h, 54h

In the Manual Configuration mode, PnP registers can be accessed by the host without PnP protocol. Right after OPL3-SA3 is switched to the Manual Configuration mode, set "81h" in CSN register automatically to put OPL3-SA3 in 'Sleep' State. And when "81h" is written to Wake [CSN], it becomes possible to access to Configuration register of each logical device from the host.

To return from the Manual Configuration mode to PnP auto-configuration mode, the Wait for Key command should be sent.

Note:

The Manual Configuration mode can not be used in the system with more than one OPL3-SA3's card installed in the ISA slot.

3. Download Resource data

When OPL3-SA3 is in the Configuration state, the host can download the resources data to EEPROM and internal SRAM via 20h: Resource Data Write. To switch OPL3-SA3 into configuration mode, there are two methods.

First method is to use the normal PnP protocol. After CSN was assigned for all ISA cards by PnP software, get CSN from CM (configuration manager) and write the CSN to Wake [CSN], then OPL3-SA3 switches into configuration state.

Second method is to use the YAMAHA Key sequence which is described in the Manual Configuration mode section. After OPL3-SA3 detects YAMAHA key, OPL3-SA3 switches into the Sleep state. Writing "81h" to Wake [CSN] register changes OPL3-SA3 into Configuration state.

After OPL3-SA3 switches into the Configuration state, download the Resource data to EEPROM and internal SRAM by using following sequence.

1. Write "01h"(RDWE bit = "1") to 21h: Resource Data Write Enable register to reset internal address counter and to enable downloading the data.
2. Write Resource data to 20h: Resource Data Write register until downloading data is completed.
3. Write "00h" to 21h: Resource Data Write Enable register to disable downloading .

Note) When RDWE bit is "1", do not access to the other device.

4. External EEPROM

The resource data information of OPL3-SA3 used for PnP auto configuration is stored in external EEPROM. And either 256 x 16-bit EEPROM or 128 x 16-bit EEPROM, such as 93C55, 93C56, 93C65, 93C66 should be used.

5. Hardware Volume Control

5-1. Hardware Volume up/down/mute Control

Two digital input pins; /VOLUP and /VOLDW can control the master volume of OPL3-SA3.

When /VOLUP is low level, register value of master volume is decremented(-1). When the value reaches to "00h"(max.0dB), the input signal will not be effective.

When /VOLDW is low level, register value of master volume is incremented(+1). When the value reaches to "0Fh"(min.-30dB), the input signal will not be effective.

When both of the /VOLUP and /VOLDW are low level simultaneously, volume is muted. When either /VOLUP or /VOLDW is low level, the previous value becomes effective, and volume is no mute.

5-2. Hardware Volume Interrupt

If configured VEN(Hardware Volume Enable)=1, SA3 Control Register, index 0Ah, D7 bit, when one of the hardware volume control pins /VOLUP or /VOLDW is asserted or when both are asserted to request mute, interrupt will be posted in the interrupt channel specified in SA3 Control Register, index 17h, IRQ-A MV or IRQ-B MV bit.

Note that when the muting is in effect, the subsequent mute requests which does not change any register contents WILL generate interrupts. The ignored UP/DOWN requests (UP requests with 0dB Volume attn., DOWN requests with -30dB) will NOT generate interrupts.

This bit is cleared upon host's reading the Master Volume Lch register, SA3 Control Register, index 07h.

6. DAC interface

OPL3-SA3 supports two types of DAC interface format. One is the conventional DAC interface format (very common for the consumer audio product) for OPL4-ML. Another is the I²S format for Zoomed Video port.

These two types of the formats are shown in the following Fig.6-1,2.

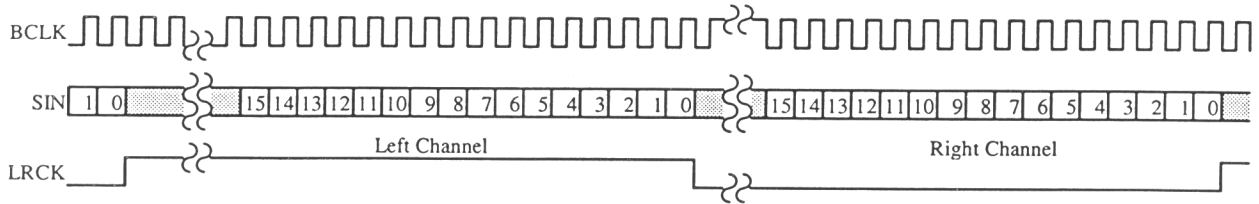


Fig.6-1 Conventional DAC Interface Format for OPL4-ML

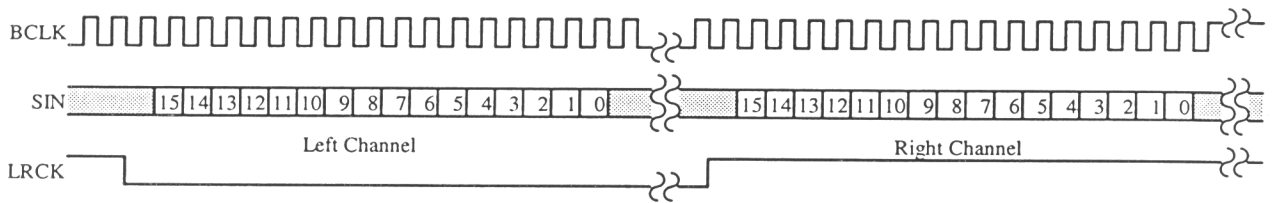


Fig.6-2 I²S Format for Zoomed Video Port

7. 3D Enhanced Control

OPL3-SA3 integrates the 3D enhanced controller including all the analog components in conventional systems. Wide, bass, and treble controls are available via SA3 control register, index 14h, 15h, 16h.

Following diagram(Fig.7-1) shows the 3D enhanced controller sub-system.

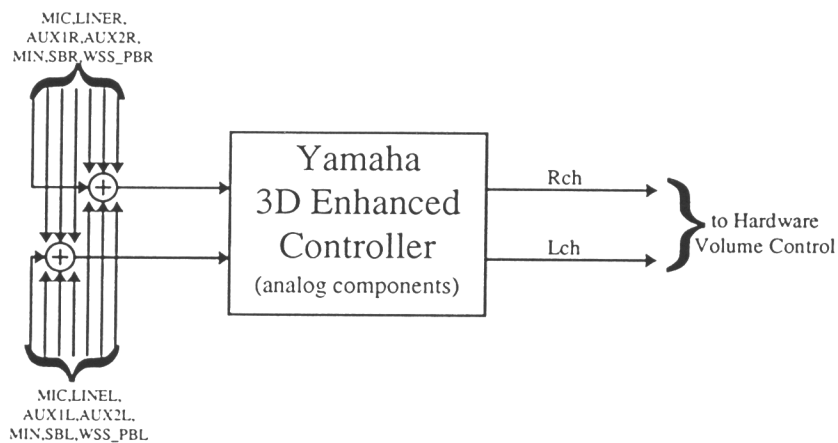
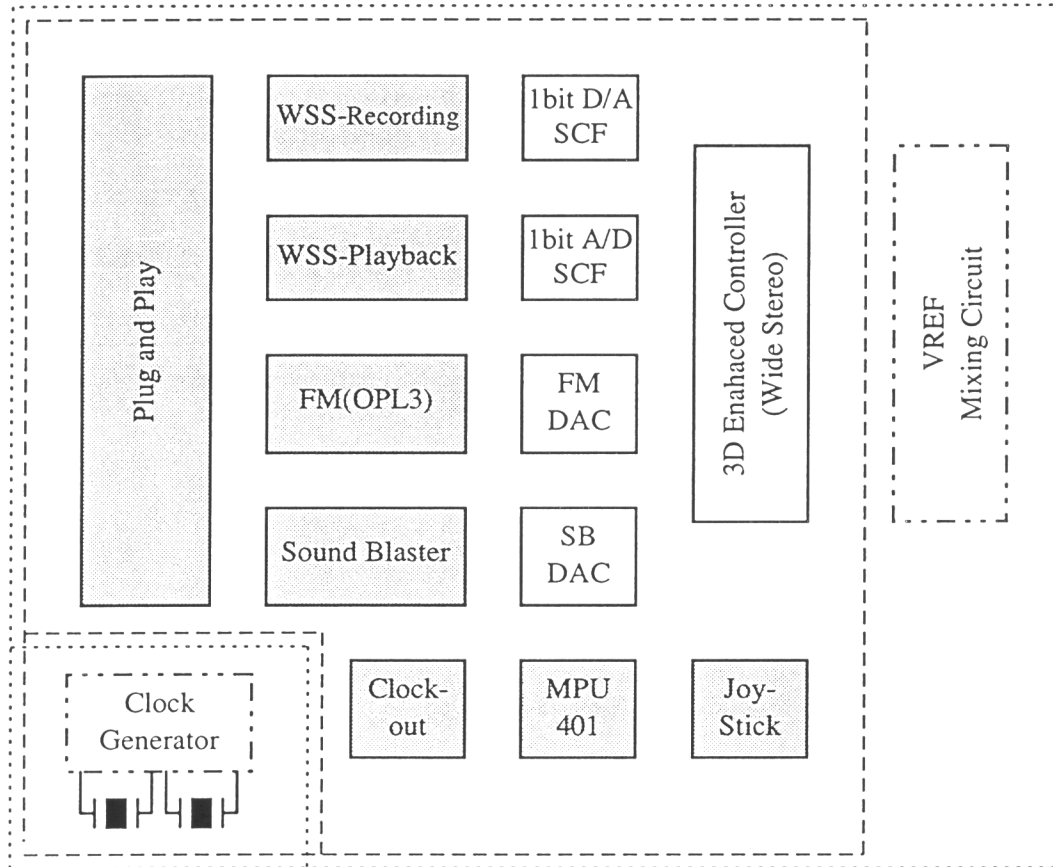


Fig.7-1 3D Enhanced Control Block Diagram

8. Power Management

Following 4 functionalities are provided for APM(Advanced Power Management) compliance.

- (1) Partial Power Down Mode
- (2) Power Save Mode
- (3) Global Power Down Mode
- (4) Suspend/Resume Mode




- : Global Power Down
- : Power Save 1,2
- : Partial Power Down (digital) : 8 digital blocks can be disabled independently.
- : Partial Power Down (analog) : 5 analog blocks can be disabled independently.

Fig.8-1 Power Management

8-1. Partial Power Down Mode

Functional blocks comprising OPL3-SA3 which are shown in Fig.8-1, are designed so they can be disabled independent of each other. SA3 control register, index 12h and 13h, implements these controls (see section 9-1-5).

 blocks in the above diagram show those that can be disabled/enabled. Note, however, the OPL3-SA3 dissipates more power with all these blocks “partial power down”ed than that can be achieved in “power save mode 2”.

In this mode, master volume is not muted, so all analog input sources and enabled digital sources (i.e. FM, SB, WSS etc.) can be heard.

Note:

AUX2 inputs are exceptions in this regard since setting FM-DAC at index 13h of SA3 Control Register inhibits the inputs altogether.

8-2. Power Save Mode

SA3 control register, index 01h, PSV and PDX bits, implement these controls.

Clock generator can be controlled under either two options.

(i) Power Save Mode 1 (Clock Generator Control : Disabled (stop)) (PSV=PDX=1)

It is necessary to take some time before clock oscillation to stabilize. Power dissipation of digital portion becomes about 100uA(typ.), and that of analog portion becomes about 5mA(typ.).

(ii) Power Save Mode 2 (Clock Generator Control : Enabled (crystals keep on oscillating)) (PSV=1, PDX=0)

Leaving power save mode gets the OPL3-SA3 back into function instantly. Power dissipation of digital portion becomes about 10mA(typ.), and that of analog portion becomes about 5mA(typ.).

In these power save modes, the OUTL/R pins will keep the VREF voltage. During these modes, master volume is automatically muted, so all audio sources can not heard. After resuming from these modes, master volume is still muted.

8-3. Global Power Down Mode (PDN=PDX=1)

This mode is to minimize power dissipation by stopping all the function of OPL3-SA3. It is necessary to take some time before clock oscillation to stabilize. Total dissipation becomes about 10uA(typ.).

VREF voltage slowly decays to ground on transition into this mode, and quickly returns to VREF on transition from this mode. During this mode, master volume is automatically muted, so all audio sources can not heard. After resuming from this mode, master volume is still muted.

8-4. Suspend/Resume Mode

There is no "read only" or "hidden state" registers in OPL3-SA3. This means you can always read and save these values before power off and can set those values back in registers after reset or power on to achieve the suspend/resume capability.

Correspondence to APM

APM	OPL3-SA3	WIN(Driver)	BIOS
ON	ON	○	○
APM Enabled	Partial Power Down	○	×
APM Standby	Power Save(Down)	○	○
APM Suspend	OFF	○	○
OFF	OFF	○	○

Note) Analog Power OFF Feature

OPL3-SA3 has the special feature that the Analog power supplies can be removed from OPL3-SA3. This feature is independent of digital portion.

8-1. Partial Power Down Mode

Functional blocks comprising OPL3-SA3 which are shown in Fig.8-1, are designed so they can be disabled independent of each other. SA3 control register, index 12h and 13h, implements these controls (see section 9-1-5).

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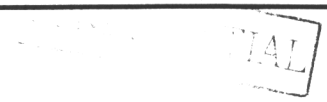
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VREF voltage slowly decays to ground on transition into this mode, and quickly returns to VREF on transition from this mode. During this mode, master volume is automatically muted, so all audio sources can not heard. After resuming from this mode, master volume is still muted.



9. Register description

9-1. SA Sound System

9-1-1. OPL3

Listed below are the OPL3-L register for AdLib compatibility.

AdLib base	(R)	Status Register port
AdLib base	(W)	Address port for Register Array 0
AdLib base + 1	(R/W)	Data port
AdLib base + 2	(W)	Address port for Register Array 1
AdLib base + 3	(R/W)	Data port

Wavetable upgrade (OPL4-ML) is available by setting /EXTEN (SEL=3, 4, 7) to "L". And, additional I/O ports listed below can also be accessed. In case of SB mode, AdLib base + 2, 3 is write only registers.

AdLib base + 4	(R)	Status port for Wavetable Register
AdLib base + 4	(W)	Address port for Wavetable Register
AdLib base + 5	(R/W)	Data port Wavetable Register
AdLib base + 6	(R/W)	reserved
AdLib base + 7	(R/W)	reserved

OPL3 Status Register (RO):

Index	D7	D6	D5	D4	D3	D2	D1	D0
xxh	IRQ	FT1	FT2	-	-	BUSY	-	BUSY

OPL3 Data Register Array 0 (R/W):

Index	D7	D6	D5	D4	D3	D2	D1	D0
00 - 01h	LSI TEST							
02h	TIMER 1							
03h	TIMER 2							
04h	RST	MT1	MT2	-	-	-	ST2	ST1
08h	-	NTS	-	-	-	-	-	-
20 - 35h	AM	VIB	EGT	KSR	MULT			
40 - 55h	KSL		TL					
60 - 75h	AR				DR			
80 - 95h	SL				RR			
A0 - A8h	F-NUM (L)							
B0 - B8h	-	-	KON	BLOCK			F-NUM (H)	
BDh	DAM	DVB	RHY	BD	SD	TOM	TC	HH
C0 - C8h	*	*	CHR	CHL	FB			CNT
E0 - F5h	-	-	-	-	-	WS		

OPL3 Data Register Array 1 (R/W)

Index	D7	D6	D5	D4	D3	D2	D1	D0
00 - 01h	LSI TEST							
04h	-	-	CONNECTION SEL					
05h	-	-	-	-	-	*	*	NEW
20 - 35h	AM	VIB	EGT	KSR	MULT			
40 - 55h	KSL		TL					
60 - 75h	AR				DR			
80 - 95h	SL				RR			
A0 - A8h	F-NUM (L)							
B0 - B8h	-	-	KON	BLOCK			F-NUM (H)	
C0 - C8h	*	*	CHR	CHL	FB			CNT
E0 - F5h	-	-	-	-	-	WS		

The bit remarked * indicates that these can be read and written but not effective.

9-1-2. Sound Blaster Pro compatibility

The followings are the I/Os for Sound Blaster Pro compatibility.

SB base	(R)	OPL3 Status port
SB base	(W)	OPL3 Address port for Register Array 0
SB base + 1h	(R/W)	OPL3 Data register
SB base + 2h	(W)	OPL3 Address port for Register Array 1
SB base + 3h	(R/W)	OPL3 Data port
SB base + 4h	(W)	SB Mixer Address port
SB base + 5h	(R/W)	SB Mixer Data port
SB base + 6h	(W)	DSP Reset port
SB base + 8h	(R)	OPL3 Status port
SB base + 8h	(W)	OPL3 Address port for Register Array 0
SB base + 9h	(R/W)	OPL3 Data port
SB base + Ah	(R)	DSP Read Data port
SB base + Ch	(R)	DSP Write-buffer status port
SB base + Ch	(W)	DSP Write Command/Data port
SB base + Eh	(R)	DSP Read-buffer status port



9-1-2-1. DSP Command

Listed below are the supported commands of DSP defined Sound Blaster Pro compatibility.

CMD	Support	Function
10h	o	8bit direct mode digitized sound I/O output
14h	o	8bit single-cycle DMA mode digitized sound output
16h	*	8bit to 2bit ADPCM single-cycle DMA mode digitized sound output
17h	*	8bit to 2bit ADPCM single-cycle DMA mode digitized sound output with ref. byte
1Ch	o	8bit auto-init DMA mode digitized sound output
1Fh	*	8bit to 2bit ADPCM auto-init DMA mode digitized sound output with ref. byte
20h	*	8bit direct mode single byte digitized sound input
24h	*	8bit single-cycle DMA mode digitized sound input
2Ch	*	8bit auto-init DMA mode digitized sound input
30h	*	Polling mode MIDI input
31h	*	Interrupt mode MIDI input
34h	*	UART polling mode MIDI I/O
35h	*	UART interrupt mode MIDI I/O
36h	*	UART polling mode MIDI I/O with time stamping
37h	*	UART interrupt mode MIDI I/O with time stamping
38h	*	MIDI output
40h	o	Set digitized sound transfer Time Constant
48h	o	Set DSP block transfer size
74h	o	8bit to 4bit ADPCM single-cycle DMA mode digitized sound output
75h	o	8bit to 4bit ADPCM single-cycle DMA mode digitized sound output with ref. byte
76h	*	8bit to 3bit ADPCM single-cycle DAM mode digitized sound output
77h	*	8bit to 3bit ADPCM single-cycle DMA mode digitized sound output with ref. byte
7Dh	o	8bit to 4bit ADPCM auto-init DMA mode digitized sound output with ref. byte
7Fh	*	8bit to 3bit ADPCM auto-init DMA mode digitized sound output with ref. byte
80h	o	Pause DAC for a duration
90h	o	8bit high-speed auto-init DMA mode digitized sound output
91h	o	8bit high-speed single-cycle DMA mode digitized sound output
98h	*	8bit high-speed auto-init DMA mode digitized sound input
99h	*	8bit high-speed single-cycle DMA mode digitized sound input
A0h	*	Set input mode to mono
A8h	*	Set input mode to stereo
D0h	o	Pause 8bit DMA mode digitized sound I/O
D1h	*	Turn on speaker
D3h	*	Turn off speaker
D4h	o	Continue 8bit DMA mode digitized sound I/O
D8h	*	Get speaker status
DAh	o	Exit 8bit auto-init DMA mode digitized sound I/O
E1h	o	Get DSP version number

Note:

- 1) The commands marked "*" are performed in state-machine, but they are not effective.
- 2) Additional undocumented commands are included.

9-1-2-2. Sound Blaster Pro compatibility Mixer

The table below is the register map of mixer of Sound Blaster Pro compatibility.

Index	D7	D6	D5	D4	D3	D2	D1	D0
00h	Reset Mixer							
04h	Voice Vol. Lch			-	Voice Vol. Rch			
0Ah	-	-	-	-	-	MIC Vol.		-
0Ch	-	-	Input Filter	-	Low Pass Filter	Input Source		-
0Eh	-	-	Output Filter	-	-	-	Stereo SW	-
22h	Master Vol. Lch			-	Master Vol. R			-
26h	MIDI Vol. Lch			-	MIDI Vol. Rch			-
28h	CD Vol. Lch			-	CD Vol. Rch			-
2Eh	Line Vol. Lch			-	Line Vol. Rch			-

The bit remarked  indicates that these can be read and written but not effective.

The actual value written to the Master Vol.,MIDI Vol.,CD Vol. and Line Vol. is based on the table shown below. And when read, actual value cannot be read and written value to each register is read instead.

		Voice Vol. (04h), CD Vol. (28h), Line Vol. (2Eh)							
		0	1	2	3	4	5	6	7
Master Volume (22h)	0	mute	mute	mute	mute	mute	mute	mute	mute
	1	mute	-28.5dB	-22.5dB	-16.5dB	-10.5dB	-7.5dB	-3.0dB	0dB
	2	mute	-22.5dB	-16.5dB	-10.5dB	-7.5dB	-3.0dB	0dB	0dB
	3	mute	-16.5dB	-10.5dB	-7.5dB	-3.0dB	0dB	0dB	0dB
	4	mute	-10.5dB	-7.5dB	-3.0dB	0dB	0dB	0dB	0dB
	5	mute	-7.5dB	-3.0dB	0dB	0dB	0dB	0dB	0dB
	6	mute	-3.0dB	0dB	0dB	0dB	0dB	0dB	0dB
	7	mute	0dB	0dB	0dB	0dB	0dB	0dB	0dB

9-1-2-1. DSP Command

Listed below are the supported commands of DSP defined Sound Blaster Pro compatibility.



CMD	Support	Function
10h	o	8bit direct mode digitized sound I/O output
14h	o	8bit single-cycle DMA mode digitized sound output
16h	*	8bit to 2bit ADPCM single-cycle DMA mode digitized sound output
17h	*	8bit to 2bit ADPCM single-cycle DMA mode digitized sound output with ref. byte
1Ch	o	8bit auto-init DMA mode digitized sound output
1Fh	*	8bit to 2bit ADPCM auto-init DMA mode digitized sound output with ref. byte
20h	*	8bit direct mode single byte digitized sound input
24h	*	8bit single-cycle DMA mode digitized sound input
2Ch	*	8bit auto-init DMA mode digitized sound input
30h	*	Polling mode MIDI input
31h	*	Interrupt mode MIDI input
34h	*	UART polling mode MIDI I/O
35h	*	UART interrupt mode MIDI I/O
36h	*	UART polling mode MIDI I/O with time stamping
37h	*	UART interrupt mode MIDI I/O with time stamping
38h	*	MIDI output
40h	o	Set digitized sound transfer Time Constant
48h	o	Set DSP block transfer size
74h	o	8bit to 4bit ADPCM single-cycle DMA mode digitized sound output
75h	o	8bit to 4bit ADPCM single-cycle DMA mode digitized sound output with ref. byte
76h	*	8bit to 3bit ADPCM single-cycle DAM mode digitized sound output
77h	*	8bit to 3bit ADPCM single-cycle DMA mode digitized sound output with ref. byte
7Dh	o	8bit to 4bit ADPCM auto-init DMA mode digitized sound output with ref. byte
7Fh	*	8bit to 3bit ADPCM auto-init DMA mode digitized sound output with ref. byte
80h	o	Pause DAC for a duration
90h	o	8bit high-speed auto-init DMA mode digitized sound output
91h	o	8bit high-speed single-cycle DMA mode digitized sound output
98h	*	8bit high-speed auto-init DMA mode digitized sound input
99h	*	8bit high-speed single-cycle DMA mode digitized sound input
A0h	*	Set input mode to mono
A8h	*	Set input mode to stereo
D0h	o	Pause 8bit DMA mode digitized sound I/O
D1h	*	Turn on speaker
D3h	*	Turn off speaker
D4h	o	Continue 8bit DMA mode digitized sound I/O
D8h	*	Get speaker status
DAh	o	Exit 8bit auto-init DMA mode digitized sound I/O
E1h	o	Get DSP version number

Note:

- 1) The commands marked "*" are performed in state-machine, but they are not effective.
- 2) Additional undocumented commands are included.

		MIDI Vol. (26h)							
		0	1	2	3	4	5	6	7
Master Volume (22h)	0	mute	mute	mute	mute	mute	mute	mute	mute
	1	mute	-24.0dB	-18.0dB	-12.0dB	-6.0dB	-3.0dB	+1.5dB	+4.5dB
	2	mute	-18.0dB	-12.0dB	-6.0dB	-3.0dB	+1.5dB	+4.5dB	+4.5dB
	3	mute	-12.0dB	-6.0dB	-3.0dB	+1.5dB	+4.5dB	+4.5dB	+4.5dB
	4	mute	-6.0dB	-3.0dB	+1.5dB	+4.5dB	+4.5dB	+4.5dB	+4.5dB
	5	mute	-3.0dB	+1.5dB	+4.5dB	+4.5dB	+4.5dB	+4.5dB	+4.5dB
	6	mute	+1.5dB	+4.5dB	+4.5dB	+4.5dB	+4.5dB	+4.5dB	+4.5dB
	7	mute	+4.5dB	+4.5dB	+4.5dB	+4.5dB	+4.5dB	+4.5dB	+4.5dB

Mixer register

SB Mixer		WSS Mixer
MIDI Vol.	→	AUX2 Vol.
CD Vol.	→	AUX1 Vol.
Line Vol.	→	Line Vol.

default

SB Mixer

Master Vol.	=	(99h)
MIDI Vol.	=	+4.5dB (99h)
Voice Vol.	=	0dB (99h)
CD Vol.	=	mute (11h)
Line Vol.	=	mute (11h)

WSS Mixer

AUX2 Vol.	=	+4.5dB (05h)
AUX1 Vol.	=	mute (88h)
Voice Vol.	=	mute (80h)
Line Vol.	=	mute (88h)
Mono Vol.	=	mute(MIN, MOUT) (C0h)

SA3 CTRL

Master Vol.	=	-14dB (07h)
MIC Vol.	=	mute (88h)

9-1-3. WSS compatible 16-bit CODEC

The followings are the I/Os for Window Sound System compatibility.

WSS base	(R)	WSS Configuration Register port
WSS base + 3h	(R)	WSS Status Register port
WSS base + 4h	(R/W)	WSS CODEC Index address port
WSS base + 5h	(R/W)	WSS CODEC Index data port
WSS base + 6h	(R/W)	WSS CODEC Status port
WSS base + 7h	(R/W)	WSS CODEC PIO Data port

WSS Configuration Register (RO):

port	D7	D6	D5	D4	D3	D2	D1	D0
+0h	"0"	"0"	IRQ			DMA		

This register is used to indicate what resources is assigned and it is read only register.

IRQ:

- "0": No interrupt channel is available
- "1": IRQ7 is available
- "2": IRQ9 is available
- "3": IRQ10 is available
- "4": IRQ11 is available
- "5"- "7": reserved.

DMA:

- "0": No DMA channel is available
- "1": DMA0
- "2": DMA1
- "3": DMA3
- "4"- "7": reserved

Notice)

In the case that CODEC is in Dual DMA mode, only playback DMA channels are valid and recording DMA channels are ignored.

WSS Status Register (RO):

port	D7	D6	D5	D4	D3	D2	D1	D0
+03h	SBHC	"0"	"04h"					

WSS CODEC Direct Registers (R/W):

port	D7	D6	D5	D4	D3	D2	D1	D0
+4h	INIT	MCE	TRD	Index Address				
+5h	Index Data							
+6h	CU/L	CL/R	CRDY	SER	PU/L	P/R	PRDY	INT
+7h	PIO Data							

WSS CODEC Indirect Registers (R/W):

Index	D7	D6	D5	D4	D3	D2	D1	D0
00h	LSS1	LSS0	LMGE	-	LIG3	LIG2	LIG1	LIG0
01h	RSS1	RSS0	RMGE	-	RIG3	RIG2	RIG1	RIG0
02h	LX1M	-	-	LX1G4	LX1G3	LX1G2	LX1G1	LX1G0
03h	RX1M	-	-	RX1G4	RX1G3	RX1G2	RX1G1	RX1G0
04h	LX2M	-	-	LX2G4	LX2G3	LX2G2	LX2G1	LX2G0
05h	RX2M	-	-	RX2G4	RX2G3	RX2G2	RX2G1	RX2G0
06h	LOM	-	LOA5	LOA4	LOA3	LOA2	LOA1	LOA0
07h	ROM	-	ROA5	ROA4	ROA3	ROA2	ROA1	ROA0
08h	FM1	FM0	C/L	S/M	CFS2	CFS1	CFS0	CSL
09h	CPIO	PPIO	-	-	ACAL	SDC	CEN	PEN
0Ah	XTL1*	XTL0*	-	-	-	-	IEN	-
0Bh	COR	PUR	ACI	DRS	"0"	"0"	"0"	"0"
0Ch	MID	MODE	-	-	ID3	ID2	ID1	ID0
0Dh	LBA5	LBA4	LBA3	LBA2	LBA1	LBA0	-	LBE
0Eh	PUB7	PUB6	PUB5	PUB4	PUB3	PUB2	PUB1	PUB0
0Fh	PLB7	PLB6	PLB5	PLB4	PLB3	PLB2	PLB1	PLB0
10h	OLB	TE	CMCE	PMCE	-	-	-	DACZ
11h	-	-	-	-	-	-	-	HPF*
12h	LLM	-	-	LLG4	LLG3	LLG2	LLG1	LLG0
13h	RLM	-	-	RLG4	RLG3	RLG2	RLG1	RLG0
14h	TL7	TL6	TL5	TL4	TL3	TL2	TL1	TL0
15h	TU7	TU6	TU5	TU4	TU3	TU2	TU1	TU0
16h	-	-	-	-	-	-	-	-
17h	-	-	-	-	-	-	-	-
18h	-	TI	CI	PI	CU	CO	PO	PU
19h	V2	V1	V0	-	-	CID2	CID1	CID0
1Ah	MIM	-	-	-	MIA3	MIA2	MIA1	MIA0
1Bh	-	-	-	-	-	-	-	-
1Ch	FMT1	FMT0	C/L	S/M	-	-	-	-
1Dh	-	-	-	-	-	-	-	-
1Eh	CUB7	CUB6	CUB5	CUB4	CUB3	CUB2	CUB1	CUB0
1Fh	CLB7	CLB6	CLB5	CLB4	CLB3	CLB2	CLB1	CLB0

The bit remarked * indicates that these can be read and written but not effective.

Mixer default:

- 02h:AUX1L = 88h (mute)
- 03h:AUX1R = 88h (mute)
- 04h:AUX2L = 05h (+4.5dB)
- 05h:AUX2R = 05h (+4.5dB)
- 06h:DACL = 80h (mute)
- 07h:DACR = 80h (mute)
- 12h:LineL = 88h (mute)
- 13h:LineR = 88h (mute)
- 1Ah:MonoIn = C0h (mute)

9-1-4. MPU401

The followings are the I/Os for MPU401 compatibility.

MPU base	(R/W)	MIDI Data port
MPU base +1	(R)	Status Register port
MPU base + 1	(W)	Command Register port

9-1-5. OPL3-SA3 control register

This register is used to control the additional functions (ex. power management, wide stereo).

CTRL base	(R/W)	Index port
CTRL base +1	(R/W)	Data port

Power Management (R/W):

Index	D7	D6	D5	D4	D3	D2	D1	D0
01h	"0"	"0"	ADOWN	"0"	"0"	PSV	PDN	PDX

ADOWN (Analog Down)... Analog power supplies can be removed from OPL3-SA3, if ADOWN="1".

Set this bit to "0", before analog power is supplied again.

PSV (power save)...

Setting this bit to "1" makes OPL3-SA3 in power save mode that is categorized into two types.

Power save mode 1

where PSV=PDX="1", clock oscillation is disabled and power dissipation of digital portion becomes about 100uA(typ.), and that of analog portion becomes about 5mA(typ.).

Power save mode 2

where PSV="1" and PDX=0, clock oscillation is active. However power dissipation of digital portion becomes about 10mA(typ.), and that of analog portion becomes about 5mA(typ.).

PDN (Power down)...

Setting this bit to "1" makes in power down mode.

PDX (Oscillation stop)...

Setting this bit to "1" makes the clock oscillation halt.

default:00h

Notice)

- 1) Set D7, D6, D4 and D3 bits to "0".
- 2) In the power save modes 1, 2, the OUTL/R pins will keep the VREF voltage. In the power down mode, VREF voltage slowly decays to ground on transition into this mode, and quickly returns to VREF on transition from this mode. During these modes (power save/down), master volume is automatically muted, so all audio sources cannot be heard. After resuming these modes, master volume is still muted.
- 3) The Joystick portion must be re-initialized by writing any value to the Joystick port after resuming from the power down/save mode.

System control (R/W):

Index	D7	D6	D5	D4	D3	D2	D1	D0
02h	SBHE	-	"0"	"0"	-	IDSEL1	IDSEL0	VZE

SBHE...

When AT-bus is used, set to "0" and set to "1" in case of XT-bus.

IDSEL1, IDSEL0...

These two bits specify the DSP version of Sound Blaster compatible portion.

The different return value of DSP command E1h (Get DSP version number) of Sound Blaster Pro is got by these bits in.

IDSEL1	IDSEL0	1st byte (major ver)	2nd byte (minor ver)
0	0	03h	01h
0	1	02h	01h
1	0	01h	05h
1	1	00h	00h

VZE...

I²S audio format can be fed to BCLK_ZV, LRCK_ZV, SIN_ZV pins of OPL3-SA3 by setting this bit to "1" regardless of the /EXTEN, when Zoomed Video port is in use.

default:00h

Notice)

Set D5 and D4 bits to "0".

Input signals, BCLK_ZV and LRCK_ZV pins which appear on SEL=4 or 5 mode, should be oscillated, when VZE=1.

Interrupt Channel configuration (R/W):

Index	D7	D6	D5	D4	D3	D2	D1	D0
03h	IRQ-B				IRQ-A			
	OPL3	MPU	SB	WSS	OPL3	MPU	SB	WSS

There are four devices (WSS (Windows Sound System CODEC), SB (Sound Blaster compatible portion), OPL3, MPU (MPU401)) that can be an interrupt source. This register specifies what interrupt source is routed to two physical interrupt (IRQA and IRQB) of OPL3-SA3. The device written to "1" is assigned to the corresponding interrupt. And by writing all "1" to upper or lower half byte, it is possible to share all interrupt sources to a single physical interrupt line.

default:69h

IRQ-A: WSS + OPL3

IRQ-B: SB + MPU401

Notice)

Do not assign a device to both IRQA and IRQB.

Interrupt (IRQ-A) status (RO):

Index	D7	D6	D5	D4	D3	D2	D1	D0
04h	-	MV	OPL3	MPU	SB	TI	CI	PI

This register is the status register that indicates which is the interrupt source of IRQA. When an interrupt occurs, the corresponding bit becomes "1" and its flag (except MV bit) is cleared when the interrupt routine is completed. This register is not cleared by writing to this register.

MV... Hardware Volume Interrupt Flag : If configured VEN=1(index 0Ah, D7 bit), the interrupt occurs when either /VOLUP or /VOLDW is low level or when both are low level to request mute. The interrupt will be posted in the IRQ-A channel, if IRQ-A MV=1 (index 17h, D4 bit).

Note that when the muting is in effect, the subsequent mute requests which does not change any register contents WILL generate interrupts. The ignored UP/DOWN requests (UP requests with 0dB Volume attn., DOWN requests with -30dB) will NOT generate interrupts.

This bit is cleared upon host's reading the Master Volume Lch register at index 07h.

OPL3... Internal FM-synthesizer Timer Flag : Note that this flag will become undefined for the configurations (SEL=3,4,7) using external synthesizer (i.e. OPL4-ML).

MPU... MPU401 Interrupt Flag

SB... Sound Blaster compatible Playback Interrupt Flag

TI... Timer Flag of CODEC

CI... Recording Flag of CODEC

PI... Playback Flag of CODEC

Notice)

- 1) Set D7, D6, D4 and D3 bits to "0".
- 2) In the power save modes 1, 2, the OUTL/R pins will keep the VREF voltage. In the power down mode, VREF voltage slowly decays to ground on transition into this mode, and quickly returns to VREF on transition from this mode. During these modes (power save/down), master volume is automatically muted, so all audio sources cannot be heard. After resuming these modes, master volume is still muted.
- 3) The Joystick portion must be re-initialized by writing any value to the Joystick port after resuming from the power down/save mode.

System control (R/W):

Index	D7	D6	D5	D4	D3	D2	D1	D0
02h	SBHE	-	"0"	"0"	-	IDSEL1	IDSEL0	VZE

SBHE...

When AT-bus is used, set to "0" and set to "1" in case of XT-bus.

IDSEL1, IDSEL0...

These two bits specify the DSP version of Sound Blaster compatible portion.

The different return value of DSP command E1h (Get DSP version number) of Sound Blaster Pro is got by these bits in.

IDSEL1	IDSEL0	1st byte (major ver)	2nd byte (minor ver)
0	0	03h	01h
0	1	02h	01h
1	0	01h	05h
1	1	00h	00h

VZE...

I²S audio format can be fed to BCLK_ZV, LRCK_ZV, SIN_ZV pins of OPL3-SA3 by setting this bit to "1" regardless of the /EXTEN, when Zoomed Video port is in use.

default:00h

Notice)

Set D5 and D4 bits to "0".

Input signals, BCLK_ZV and LRCK_ZV pins which appear on SEL=4 or 5 mode, should be oscillated, when VZE=1.

Interrupt (IRQ-B) status (RO):

Index	D7	D6	D5	D4	D3	D2	D1	D0
05h	-	MV	OPL3	MPU	SB	TI	CI	PI

This register is the status register that indicates which is the interrupt source of IRQB. When an interrupt occurs, the corresponding bit becomes "1" and its flag (except MV bit) is cleared when the interrupt routine is completed. This register is not cleared by writing to this register.

MV... Hardware Volume Interrupt Flag : If configured VEN=1(index 0Ah, D7 bit), the interrupt occurs when either /VOLUP or /VOLDW is low level or when both are low level to request mute. The interrupt will be posted in the IRQ-B channel, if IRQ-B MV=1 (index 17h, D5 bit).

Note that when the muting is in effect, the subsequent mute requests which does not change any register contents WILL generate interrupts. The ignored UP/DOWN requests (UP requests with 0dB Volume attn., DOWN requests with -30dB) will NOT generate interrupts.

This bit is cleared upon host's reading the Master Volume Lch register at index 07h.

OPL3... Internal FM-synthesizer Timer Flag : Note that this flag will become undefined for the configurations (SEL=3,4,7) using external synthesizer (i.e. OPL4-ML).

MPU... MPU401 Interrupt Flag

SB... Sound Blaster compatible Playback Interrupt Flag

TI... Timer Flag of CODEC

CI... Recording Flag of CODEC

PI... Playback Flag of CODEC

DMA configuration (R/W):

Index	D7	D6	D5	D4	D3	D2	D1	D0
06h	DMA-B				DMA-A			
	-	SB	WSS-R	WSS-P	-	SB	WSS-R	WSS-P

There are three devices (WSS-P (Windows Sound System CODEC playback), WSS-R (Windows Sound System CODEC recording) , SB(Sound Blaster compatible playback)) that may use a DMA channel. However 2 DMA channels (DMAA and DMAB) are available at maximum, this register specifies which device is routed to the physical DMA channels. And the device written to "1" is assigned to the corresponding DMA channel.

default:61h

DMA-A: WSS-P

DMA-B: WSS-R + SB

Notice)

Do not assign a device to both DMA-A and DMA-B.

Master Volume Lch (R/W):

Index	D7	D6	D5	D4	D3	D2	D1	D0
07h	MVLM	-	-	-	MVL3	MVL2	MVL1	MVL0

This register specifies the master volume of left channel.

MVLM... Setting to "1" to this bit makes Master Volume Left Channel muted.

MVL3-0... These bits determine the attenuation level of Master Volume Left Channel by -2dB step. When all bits are set to "0", volume is maximum (0dB) and when all bits are set to "1", volume is minimum (-30dB).

default: 07h (-14dB)

Notice)

During the power on reset and power down/save mode, master volume is automatically muted, so all audio sources can not be heard. In resuming from power down/save mode, it is still muted.

Master Volume Rch (R/W):

Index	D7	D6	D5	D4	D3	D2	D1	D0
08h	MVRM	-	-	-	MVR3	MVR2	MVR1	MVR0

This register specifies the master volume of right channel.

MVRM... Setting to "1" to this bit makes Master Volume Right Channel muted.

MVR3-0... These bits determine the attenuation level of Master Volume Right Channel by -2dB step. When all bits are set to "0", volume is maximum (0dB) and when all bits are set to "1", volume is minimum (-30dB).

default: 07h (-14dB)

Notice)

During the power on reset and power down/save mode, master volume is automatically muted, so all audio sources can not be heard. In resuming from power down/save mode, it is still muted.

MIC Volume (R/W):

Index	D7	D6	D5	D4	D3	D2	D1	D0
09h	MICM	-	-	MCV4	MCV3	MCV2	MCV1	MCV0

This register specifies the master volume of MIC.

MICM... Setting to "1" to this bit makes Mic Volume muted.

MCV4-0... These bits determine the gain level of Mic volume by -1.5dB step. When all bits are set to "0", volume is maximum(+12dB) and when all bits are set to "1", volume is minimum (-34.5dB).

default:88h

Miscellaneous:

Index	D7	D6	D5	D4	D3	D2	D1	D0
0Ah	VEN	-	-	MCSW	MODE	VER2	VER1	VER0

- VEN... This bit enables the hardware volume control. Default is VEN="1".
- MCSW... This bit determines whether Rch of Mic input or loopback of monaural output is connected to A/D. This will be useful to support the echo cancellation. When "0" is set to this bit, Rch of Mic input is selected.
- MODE... This bit indicates the SB or WSS mode. If MODE=0, it is the SB mode. This bit is read only.
- VER2-0... These bits indicate the version of OPL3-SA3 and read only (VER2="0", VER1="1", VER0="0").

default:82h

WSS DMA Base counter (R/W):

Index	D7	D6	D5	D4	D3	D2	D1	D0
0Bh	Playback Base Counter (Low)							
0Ch	Playback Base Counter (High)							
0Dh	Recording Base Counter (Low)							
0Eh	Recording Base Counter (High)							

These registers are to load the value to WSS DMA base counter and read out the present value. Initial value is FFh.

In case of loading the value, both high and low bytes are loaded to internal DMA counter when the high byte is written. The value set to this register is "(the number of transfer byte) -1" that is same as WSS CODEC indirect register 0Eh, 0Fh, 1Eh and 1Fh.

When read these registers, the present value of DMA base counter is read out.

These registers are used mainly to support the suspend/resume feature that is very important for Notebook PC application.

WSS Interrupt Scan out/in (R/W):

Index	D7	D6	D5	D4	D3	D2	D1	D0
0Fh	-	-	-	-	-	STI	SCI	SPI

Use the bits in this register to set WSS interrupt-flags(WSS CODEC indirect Register, index 18h, D6-D4 bits).

STI... "1" in this bit means TI="1" and corresponding IRQ active.

SCI... "1" in this bit means CI="1" and corresponding IRQ active.

SPI... "1" in this bit means PI="1" and corresponding IRQ active.

default:00h

Notice)

To make IRQ active, it is necessary to set "1" to WSS CODEC indirect register index 0Ah IEN bit.

Sound Blaster compatibility Internal State Scan out/in (R/W):

Index	D7	D6	D5	D4	D3	D2	D1	D0
10h	SBPDA	-	-	-	SS	SM	SE	SBPDR

SBPDA... Sound Blaster Power Down Acknowledgment: "1" in SBPDA acknowledges that OPL3-SA3 is ready for scanning internal state data in/out or for power down operation. This flag is read-only.

SS... Scan Select : Set "1" in this bit when reading or writing internal state.
Set "0" for normal operation.

SM... Scan Mode : Setting "1" in this bit means the internal state's are read(out).
Set "0" for write(in).

SE... Scan Enable : "1" to "0" transition in this bit clocks the shifting internal state scan data out 1-bit at a time.

SBPDR... Sound Blaster Power Down Request : "1" in this bit inhibits further DMA requests and have the internal state begin shutdown procedure. "1" in SBPDA signals the shutdown procedure completion.

default:00h

Sound Blaster compatibility Internal State Scan Data (R/W):

Index	D7	D6	D5	D4	D3	D2	D1	D0
11h	SCAN DATA							

SCAN DATA... Data port for internal state scan data in/out.

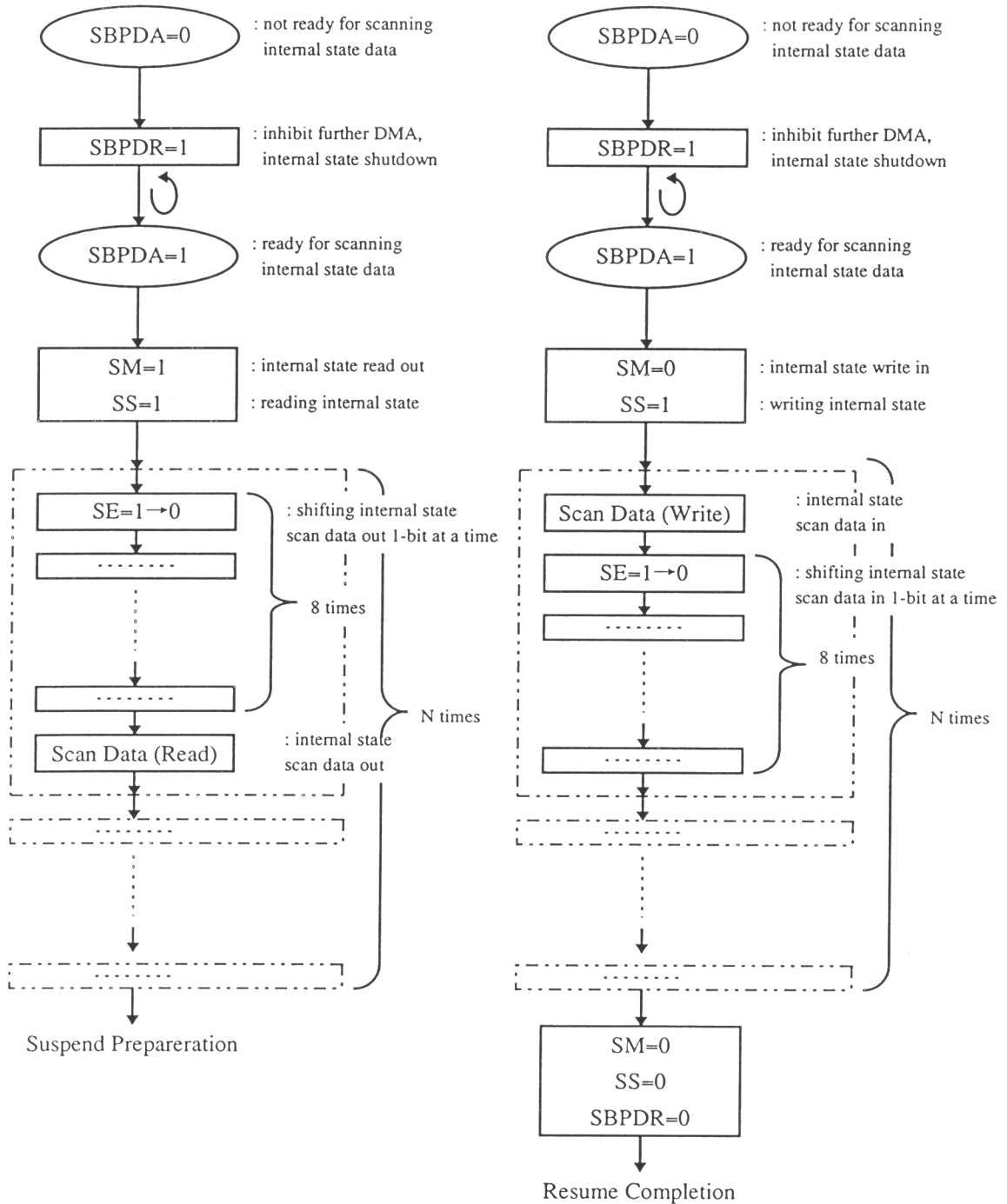
default:00h

Notice)

The Sound Blaster compatibility internal state scan out/in sequence are shown in the following Fig.9-1.

i) Scan Out

ii) Scan In



N=28 byte (Total Scan Data=218 bit(27 byte×8+2bit))

Fig. 9-1 Sound Blaster compatibility Internal State Scan out/in Sequence

Digital Block Partial Power Down (R/W):

Index	D7	D6	D5	D4	D3	D2	D1	D0
12h	JOY	MPU	MCLKO	FM	WSS_R	WSS_P	SB	PnP

This register specifies the partial power management of the digital portion. This function is to spare power dissipation in unneeded blocks.

- JOY... Setting this bit to "1" makes the Joystick portion in power down mode. Note that the Joystick portion must be re-initialized by writing any value to the Joystick port after resuming from the Joystick portion power down mode.
- MPU... Setting this bit to "1" makes the MPU401 portion in power down mode.
- MCLKO when set to "1", Master Clock(33.8688MHz) is disable, which appears on the pin MP9(SEL=1,3,4,7).
when set to "0", normal operation is active.
- FM... Setting this bit to "1" makes the internal FM(OPL3) portion in power down mode.
- WSS_R... Setting this bit to "1" makes the WSS recording portion in power down mode.
- WSS_P... Setting this bit to "1" makes the WSS playback portion and the digital loopback portion in power down mode.
- SB... Setting this bit to "1" makes the Sound Blaster compatible portion in power down mode.
- PnP... Setting this bit to "1" makes the PnP portion in power down mode.
- default:00h

Analog Block Partial Power Down (R/W):

Index	D7	D6	D5	D4	D3	D2	D1	D0
13h	-	-	-	FMDAC	A/D	D/A	SBDAC	WIDE

This register specifies the partial power management of the analog portion. The respective outputs of the blocks which are to be disabled should be muted beforehand.

- FMDAC... Setting this bit to "1" makes the FMDAC portion for the internal FM(OPL3) or external synthesizer(OPL4-ML) or ZV port etc. in power down mode. AUX2 should be muted via register before setting the FMDAC portion to power down.
- A/D... Setting this bit to "1" makes the A/D portion for the WSS recording in power down mode.
- D/A... Setting this bit to "1" makes the D/A portion for the WSS playback in power down mode. WSS CODEC indirect register, index 06h and 07h, LOM and ROM bits must be "1", before doing this.
- SBDAC... Setting this bit to "1" makes the SBDAC portion in power down mode. SB master volume should be muted via register before setting the SBDAC portion to power down.
- WIDE... Setting this bit to "1" makes the Wide Stereo(3D Enhanced Control) portion in power down mode. The 3D Enhanced parameter registers at index 14, 15, and 16h must be 00h, when doing this.
- default:00h

Notice)

In the partial power down mode, master volume is not muted, so all analog input sources and enabled digital sources (i.e. FM, SB, WSS etc.) can be heard. Note that AUX2 inputs are exceptions in this regard since setting FMDAC bit inhibits the inputs altogether.

3D Enhanced control(WIDE) (R/W):

Index	D7	D6	D5	D4	D3	D2	D1	D0
14h	-	WIDER2	WIDER1	WIDER0	-	WIDEL2	WIDEL1	WIDEL0

This register specifies the wide level of the 3D enhanced control.

WIDER2-0... These bits determine the wide level of 3D enhanced control on Right Channel by 8 step (if WIDER2-0=0, 0%, and WIDER2-0=7, 100%).

WIDEL2-0... These bits determine the wide level of 3D enhanced control on Left Channel by 8 step (if WIDEL2-0=0, 0%, and WIDEL2-0=7, 100%).

default:00h

3D Enhanced control(BASS) (R/W):

Index	D7	D6	D5	D4	D3	D2	D1	D0
15h	-	BASSR2	BASSR1	BASSR0	-	BASSL2	BASSL1	BASSL0

This register specifies the bass level of the 3D enhanced control.

BASSR2-0... These bits determine the bass level of 3D enhanced control on Right Channel by 1.5dB step(Max. 10.5dB).

BASSL2-0... These bits determine the bass level of 3D enhanced control on Left Channel by 1.5dB step(Max. 10.5dB).

default:00h

3D Enhanced control(TREBLE) (R/W):

Index	D7	D6	D5	D4	D3	D2	D1	D0
16h	-	TRER2	TRER1	TRER0	-	TREL2	TREL1	TREL0

This register specifies the treble level of the 3D enhanced control.

TRER2-0... These bits determine the treble level of 3D enhanced control on Right Channel by 1.5dB step(Max. 10.5dB).

TREL2-0... These bits determine the treble level of 3D enhanced control on Left Channel by 1.5dB step(Max. 10.5dB).

default:00h

Notice)

The 3D Enhanced control parameter registers at index 14h, 15h and 16h must be 00h, when doing the Wide Stereo portion in power down mode (setting SA3 control register, index 13h, WIDE bit to "1").

Hardware Volume Interrupt Channel Configuration (R/W):

Index	D7	D6	D5	D4	D3	D2	D1	D0
17h	-	-	IRQ-B MV	IRQ-A MV	-	*	*	*

The Hardware Volume can source interrupt. This register indicates which interrupt channel will be used. If IRQ-A MV="1", assigned to IRQ-A.

default:00h

Notice)

Writing to the other bit positions is invalid, though the bits remarked * (D2-D0) will retain written values. D3, D6 and D7 will always returns "0" when read.

9-2. Joystick

port	D7	D6	D5	D4	D3	D2	D1	D0
xxh	JBB2	JBB1	JAB2	JAB1	JBCY	JBCX	JACY	JACX

JACX... Joystick A, Coordinate X

JACY... Joystick A, Coordinate Y

JBCX... Joystick B, Coordinate X

JBCY... Joystick B, Coordinate Y

JAB1... Joystick A, Button 1

JAB2... Joystick A, Button 2

JBB1... Joystick B, Button 1

JBB2... Joystick B, Button 2

Notice)

The Joystick portion must be re-initialized by writing any value to the Joystick port after resuming from the power down/save or the Joystick portion power down mode.

9-3. MODEM

The following pins are for MODEM interface with PnP supported.

/MCS... chip select (eight consecutive byte I/O)

MIRQ... interrupt signal

And MIN is the analog input to mix the telephone line.

MIN... analog input

9-4. CD-ROM

The following pins are for IDE CD-ROM interface with PnP supported.

/CDCS0... chip select for CD-ROM

/CDCS1... chip select for CD-ROM

CDIRQ... interrupt signal

Other signals needed for CD-ROM must be generated by the external PALs, which is described in section 1-3.

■ Electrical Characteristics

Absolute Maximum Ratings

Item	Symbol	Minimum	Maximum	Unit
Power Supply Voltage (Analog/Digital)	V_{DD}	$V_{SS}-0.5$	$V_{SS}+7.0$	V
Input Voltage	V_{IN}	$V_{SS}-0.5$	$V_{DD}+0.5$	V
Output Voltage	V_{OUT}	$V_{SS}-0.3$	$V_{DD}+0.3$	V
Input Current	I_{IN}	-20	20	mA
Storage Temperature	T_{STG}	-50	125	°C

Note : $V_{DD}=DV_{DD}=AV_{DD}$, $V_{SS}=DV_{SS}=AV_{SS}=0[V]$

Recommended Operating Conditions

Item	Symbol	Min.	Typ.	Max.	Unit
Power Supply 1 (Analog)	AV_{DD}	4.75	5.00	5.25	V
5.0V Spec. (Digital)	DV_{DD}	4.75	5.00	5.25	V
Power Supply 2 (Analog)	AV_{DD}	4.75	5.00	5.25	V
3.3V Spec. (Digital)	DV_{DD}	3.00	3.30	3.60	V
Operating Ambient Temperature	T_{OP}	0	25	70	°C

Note : $DV_{SS}=AV_{SS}=0[V]$

DC Characteristics 1 ($DV_{DD} = 5.0 \pm 0.25[V]$)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
TTL-Input Pins						
High Level Input Voltage 1	V_{IH1}	Except schmitt inputs	2.0		0.8	V
Low Level Input Voltage 1	V_{IL1}					V
CMOS-Input Pins						
High Level Input Voltage 2	V_{IH2}		$0.7DV_{DD}$		$0.2DV_{DD}$	V
Low Level Input Voltage 2	V_{IL2}					V
Schmitt V_t- (H to L)	V_{t-}	*1	0.8		1.5	V
Schmitt V_t+ (L to H)	V_{t+}		1.3		2.1	V
Schmitt Hysteresis	V_{h1}		0.3			V
	V_{h2}	*2	0.1			V
Input Leakage Current	I_L	$V_{IN}=DV_{SS}$, DV_{DD}	-10		10	μA
Input Capacitance	C_I				10	pF
Pull up Register	R_{U1}	RXD	20	50	100	k Ω
	R_{U2}	GP7~4	30	100	200	k Ω
	R_{U3}	Otherwise	50	200	400	k Ω
TTL-Output Pins						
High Level Output Voltage 1	V_{OH1}	*3	2.4		0.4(0.5)	V
Low Level Output Voltage 1	V_{OL1}					V
TTL Output Current	I_{OHL1}	D7~0 pins *3	16(24)			mA
	I_{OHL2}	IRQn, DRQn pins *3	8(12)			mA
	I_{OHL3}	TXD pin	4			mA
	I_{OHL4}	MP9-0 pins	2			mA

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
CMOS Output pins						
High Level Output Voltage 2	V_{OH2}	$I_{OH}=2\text{mA}$	$0.8DV_{DD}$			V
Low Level Output Voltage 2	V_{OL2}	$I_{OL}=2\text{mA}$			0.4	V
Output Leakage Current	O_L	Hi_Z: $V_{IN}=DV_{SS}, DV_{DD}$	-10		10	μA
Output Capacitance	C_O				10	pF

Note : $DV_{SS}=AV_{SS}=0[V]$, $T_{OP}=0\sim 70^\circ\text{C}$, $AV_{DD}=5.0[V]$

*1 : Applicable to schmitt input terminals except /VOLUP and /VOLDW.

*2 : Applicable to /VOLUP and /VOLDW terminals.

*3 : When $V_{OL1}=\text{max. } 0.5\text{V}$, the value into the brackets is specified at $I_{OHL1, 2}$.

DC Characteristics 2 ($DV_{DD} = 3.3 \pm 0.30[V]$)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
TTL-Input Pins						
High Level Input Voltage 1	V_{IH1}	Except schmitt inputs	2.0			V
Low Level Input Voltage 1	V_{IL1}				0.8	V
CMOS-Input Pins						
High Level Input Voltage 2	V_{IH2}		$0.7DV_{DD}$			V
Low Level Input Voltage 2	V_{IL2}				$0.2DV_{DD}$	V
Schmitt V_t- (H to L)	V_{t-}		0.8		1.5	V
Schmitt V_t+ (L to H)	V_{t+}		1.3		2.2 *	V
Schmitt Hysteresis	V_h		0.3			V
Input Leakage Current	I_L	$V_{IN}=DV_{SS}, DV_{DD}$	-10		10	μA
Input Capacitance	C_I				10	pF
Pull up Register	R_{U1} R_{U2} R_{U3}	RXD GP7~4 Otherwise	20 30 50	50 100 200	100 200 400	k Ω k Ω k Ω
TTL-Output Pins						
High Level Output Voltage 1	V_{OH1}		2.4			V
Low Level Output Voltage 1	V_{OL1}				0.4	V
TTL Output Current	I_{OHL1} I_{OHL2} I_{OHL3} I_{OHL4}	D7~0 pins IRQn, DRQn pins TXD pin MP9-0 pins	2 * 2 * 2 * 2			mA mA mA mA
CMOS Output pins						
High Level Output Voltage 2	V_{OH2}	$I_{OH}=2\text{mA}$	$0.8DV_{DD}$			V
Low Level Output Voltage 2	V_{OL2}			$I_{OL}=2\text{mA}$		0.4
Output Leakage Current	O_L	Hi_Z: $V_{IN}=DV_{SS}, DV_{DD}$	-10		10	μA
Output Capacitance	C_O				10	pF

Note : $DV_{SS}=AV_{SS}=0[V]$, $T_{OP}=0\sim 70^\circ\text{C}$, $AV_{DD}=5.0[V]$

The specifications marked "*" are different from the value at $DV_{DD} = 5.0 \pm 0.25[V]$

AC Characteristics

CPU Interface & DMA BUS Cycle :Fig.1,2,3,4,5,6,7,8

Item	Symbol	Min.	Typ.	Max.	Unit
/DACK inactive to /IOW, /IOR falling edge	t_{AKS}	50			ns
/DACK active from /IOW, /IOR rising edge	t_{AKH}	10			ns
Address set up to /IOW, /IOR active	t_{AS}	40			ns
Address hold to /IOW, /IOR inactive	t_{AH}	10			ns
/IOW Write Pulse Width	t_{WW}	90			ns
Write Data set up to /IOW active	t_{WDS}	20			ns
Write Data hold to /IOW inactive	t_{WDH}	10			ns
/IOR Read Pulse Width	t_{RW}	90			ns
Read Data access time	t_{ACC}			80	ns
Read Data hold from /IOR inactive	t_{RDH}	0			ns
DRQ hold from /IOW, /IOR falling edge	t_{DGH}	0		20	ns
/DACK set up to /IOW, /IOR falling edge	t_{SF}	25			ns
/DACK hold to /IOW, /IOR rising edge	t_{HR}	25			ns
Time between rising edge of /IOW, /IOR to next falling edge of /IOW, /IOR	t_{NX}	100			ns
Valid Address from /SYNCS or /MCS or /CDCS1-0	t_{EX1}			150(70) *	ns
/SYNCS or /MCS or /CDCS1-0 hold to Valid Address	t_{EX2}			150(70) *	ns
RESET Pulse Width	t_{RST}	90			μ s

Note : $DV_{SS}=AV_{SS}=0[V]$, $T_{Op}=0\sim 70^{\circ}C$, $DV_{DD}=5.0\pm 0.25[V]$ or $3.3\pm 0.30[V]$, $AV_{DD}=5.0[V]$

The value into the brackets is specified at $DV_{DD}=3.3\pm 0.30[V]$.

Serial Audio (Zoomed Video) Interface Input :Fig.9

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
BCLK Cycle	f_{BCK}		32fs	48fs	64fs	kHz
BCLK Duty	D_{BCLK}		40	50	60	%
LRCK Hold Time	t_{LRH}	BCLK \uparrow /LRCK	-120		120	ns
SIN Set up Time	t_{DS}	BCLK \uparrow /SIN	20			ns
SIN Hold Time	t_{DH}	BCLK \uparrow /SIN	20			ns
CLKO Frequency	f_{CLKO33}			33.8688		MHz
CLKO Duty	D_{CLKO33}	$f_{33}=50\%$	40	50	60	%

Note : $DV_{SS}=AV_{SS}=0[V]$, $T_{Op}=0\sim 70^{\circ}C$, $DV_{DD}=5.0\pm 0.25[V]$ or $3.3\pm 0.30[V]$, $AV_{DD}=5.0[V]$

Duty Search Point is $1/2 DV_{DD}$

Miscellaneous

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Master Clock Frequency (X'tal 33) Duty	f_{33}	*1		33.8688		MHz
	D_{f33}		40	50	60	%
Master Clock Frequency (X'tal 24) Duty	f_{24}	*1		24.5760		MHz
	D_{f24}		40	50	60	%
Power Consumption 1 (Normal)	P_{OP1}	$DV_{DD}=5.0\pm 0.25[V]$		40	50	mA
		$AV_{DD}=5.0\pm 0.25[V]$		50	60	mA
	P_{OP2}	$DV_{DD}=3.3\pm 0.30[V]$		25	35	mA
Power Consumption 2 (Power Save 1)		$DV_{DD}=5.0\pm 0.25[V]$		100		μA
		$AV_{DD}=5.0\pm 0.25[V]$		5		mA
		$DV_{DD}=3.3\pm 0.30[V]$		80		μA
Power Consumption 3 (Power Save 2)		$DV_{DD}=5.0\pm 0.25[V]$		10		mA
		$AV_{DD}=5.0\pm 0.25[V]$		5		mA
		$DV_{DD}=3.3\pm 0.30[V]$		7		mA
Power Consumption 4 (Partial Power Down)		$DV_{DD}=5.0\pm 0.25[V]$		20		mA
		$AV_{DD}=5.0\pm 0.25[V]$		15		mA
		$DV_{DD}=3.3\pm 0.30[V]$		10		mA
Power Consumption 5 (Power Down)		$DV_{DD}=5.0\pm 0.25[V]$		10	40	μA
		$AV_{DD}=5.0\pm 0.25[V]$		0	10	μA
		$DV_{DD}=3.3\pm 0.30[V]$		10	30	μA

Note : $DV_{SS}=AV_{SS}=0[V]$, $T_{OP}=0\sim 70^{\circ}C$

Duty Search Point is $1/2 DV_{DD}$.

*1... $DV_{DD} = 5.0\pm 0.25[V]$ or $3.3V\pm 0.30[V]$, $AV_{DD} = 5.0\pm 0.25[V]$

Power Save 1 : SA3 Control Register, index 01h, PSV=PDX=1

Power Save 2 : SA3 Control Register, index 01h, PSV=1, PDX=0

Partial power down : SA3 Control Register, index 12h=FFh, index 13h=1Fh

Power Down : SA3 Control Register, index 01h, PDN=PDX=1

AC Characteristics

CPU Interface & DMA BUS Cycle :Fig.1,2,3,4,5,6,7,8

Item	Symbol	Min.	Typ.	Max.	Unit
/DACK inactive to /IOW, /IOR falling edge	t_{AKS}	50			ns
/DACK active from /IOW, /IOR rising edge	t_{AKH}	10			ns
Address set up to /IOW, /IOR active	t_{AS}	40			ns
Address hold to /IOW, /IOR inactive	t_{AH}	10			ns
/IOW Write Pulse Width	t_{WW}	90			ns
Write Data set up to /IOW active	t_{WDS}	20			ns
Write Data hold to /IOW inactive	t_{WDH}	10			ns
/IOR Read Pulse Width	t_{RW}	90			ns
Read Data access time	t_{ACC}			80	ns
Read Data hold from /IOR inactive	t_{RDH}	0			ns
DRQ hold from /IOW, /IOR falling edge	t_{DGH}	0		20	ns
/DACK set up to /IOW, /IOR falling edge	t_{SF}	25			ns
/DACK hold to /IOW, /IOR rising edge	t_{HR}	25			ns
Time between rising edge of /IOW, /IOR to next falling edge of /IOW, /IOR	t_{NX}	100			ns
Valid Address from /SYNCS or /MCS or /CDCS1-0	t_{EX1}			150(70) *	ns
/SYNCS or /MCS or /CDCS1-0 hold to Valid Address	t_{EX2}			150(70) *	ns
RESET Pulse Width	t_{RST}	90			μs

Note : $DV_{SS}=AV_{SS}=0[V]$, $T_{OP}=0\sim 70^{\circ}C$, $DV_{DD}=5.0\pm 0.25[V]$ or $3.3\pm 0.30[V]$, $AV_{DD}=5.0[V]$
 The value into the brackets is specified at $DV_{DD}=3.3\pm 0.30[V]$.

Serial Audio (Zoomed Video) Interface Input :Fig.9

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
BCLK Cycle	f_{BCK}		32fs	48fs	64fs	kHz
BCLK Duty	D_{BCLK}		40	50	60	%
LRCK Hold Time	t_{LRH}	BCLK \uparrow /LRCK	-120		120	ns
SIN Set up Time	t_{DS}	BCLK \uparrow /SIN	20			ns
SIN Hold Time	t_{DH}	BCLK \uparrow /SIN	20			ns
CLKO Frequency	f_{CLKO33}			33.8688		MHz
CLKO Duty	D_{CLKO33}	$f_{33}=50\%$	40	50	60	%

Note : $DV_{SS}=AV_{SS}=0[V]$, $T_{OP}=0\sim 70^{\circ}C$, $DV_{DD}=5.0\pm 0.25[V]$ or $3.3\pm 0.30[V]$, $AV_{DD}=5.0[V]$
 Duty Search Point is $1/2 DV_{DD}$

I/O Write Cycle

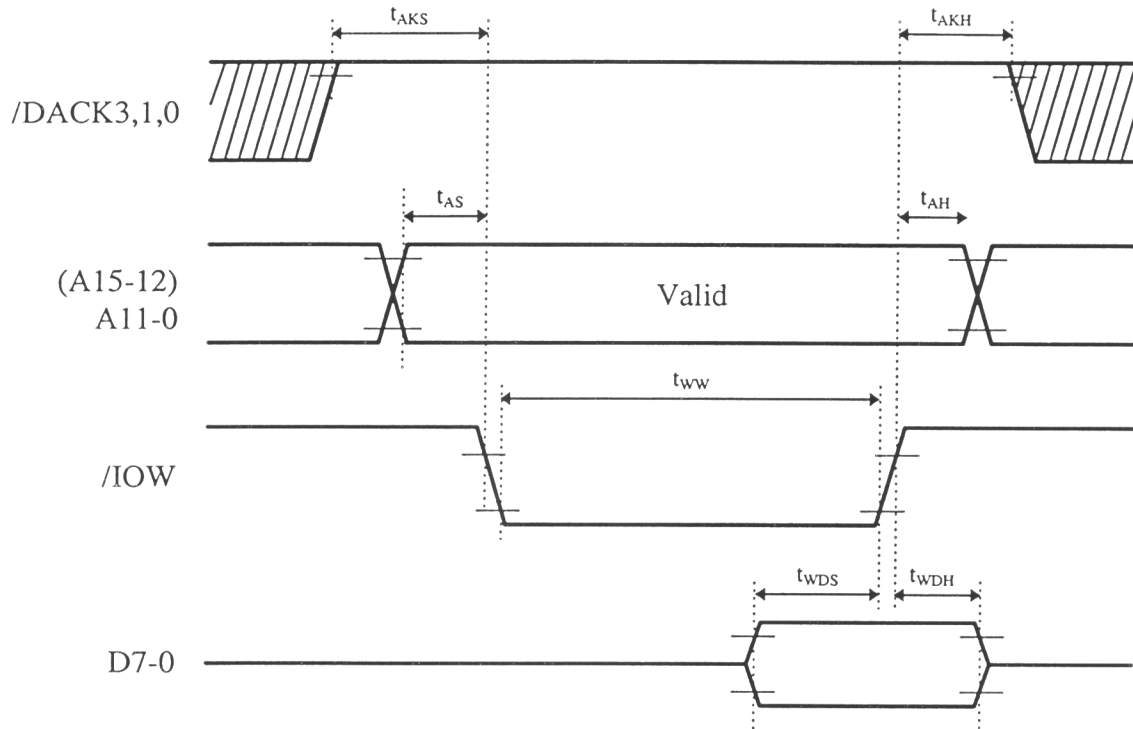


Fig.1

I/O Read Cycle

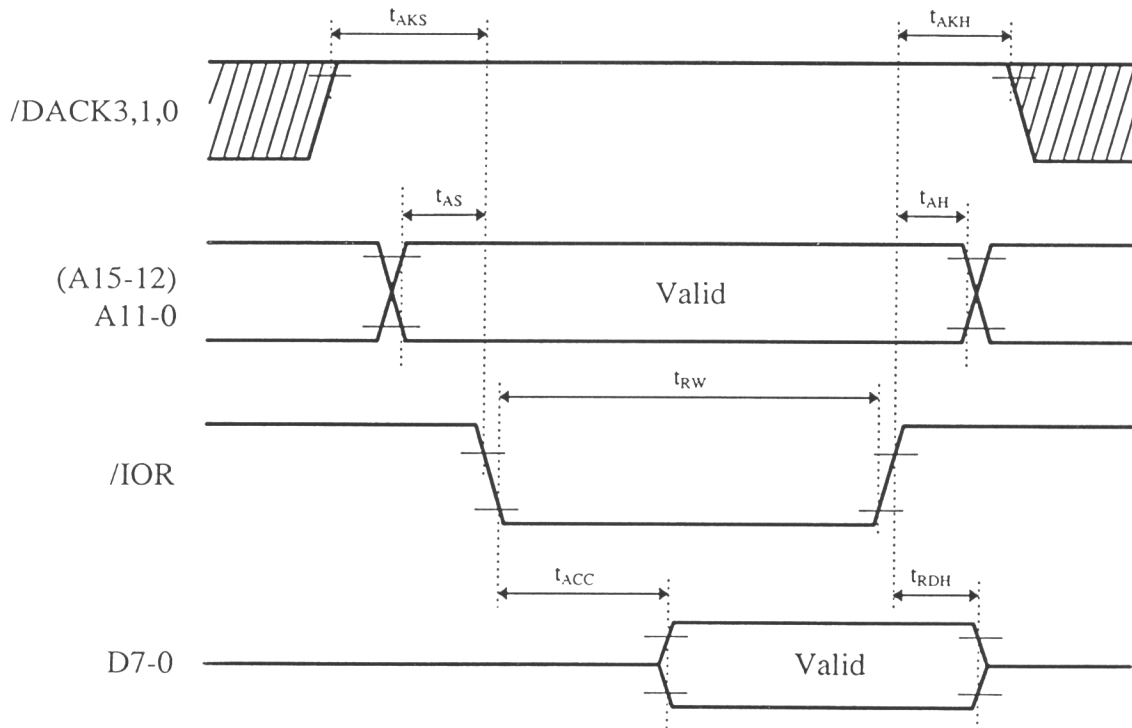


Fig.2

ORIGINAL

8bit Mono & ADPCM DMA Write Cycle

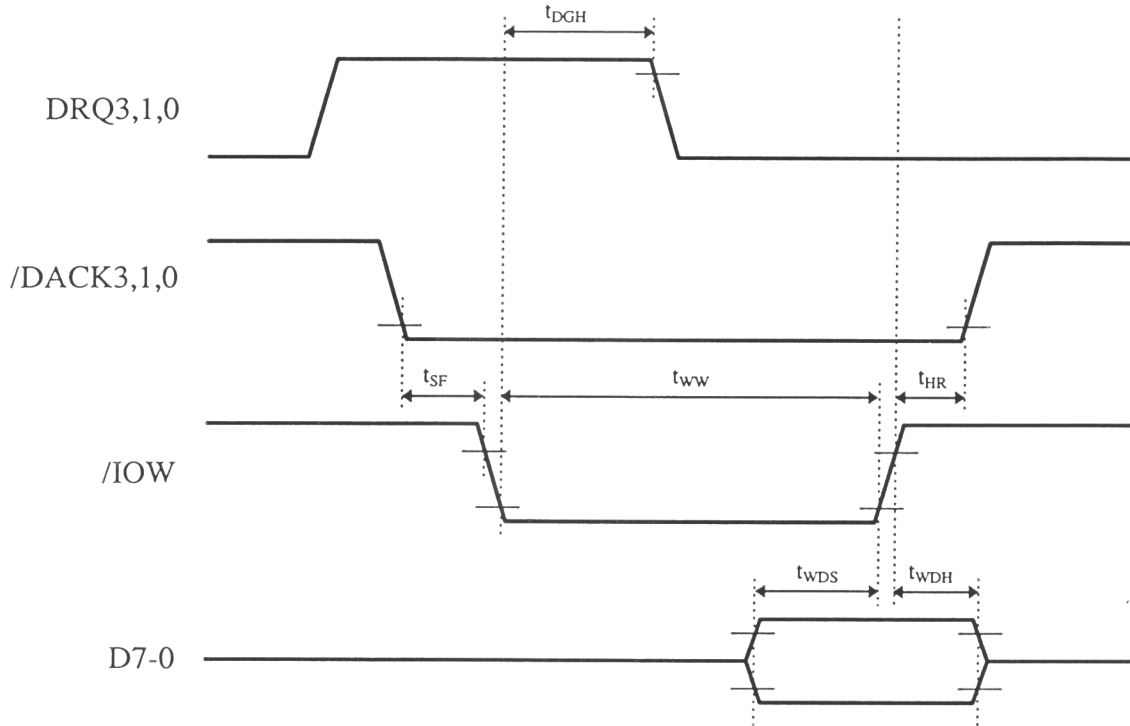


Fig.3

8bit Mono & ADPCM DMA Read Cycle

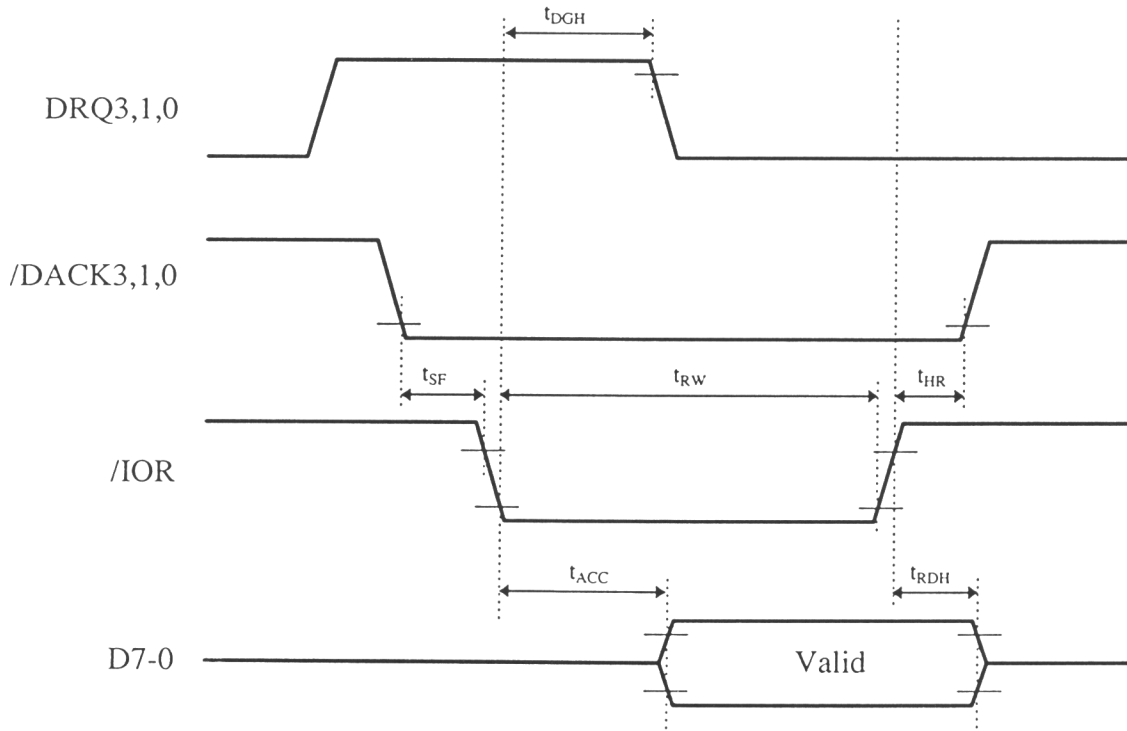
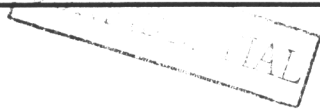


Fig.4



8bit Stereo or 16bit Mono DMA Cycle

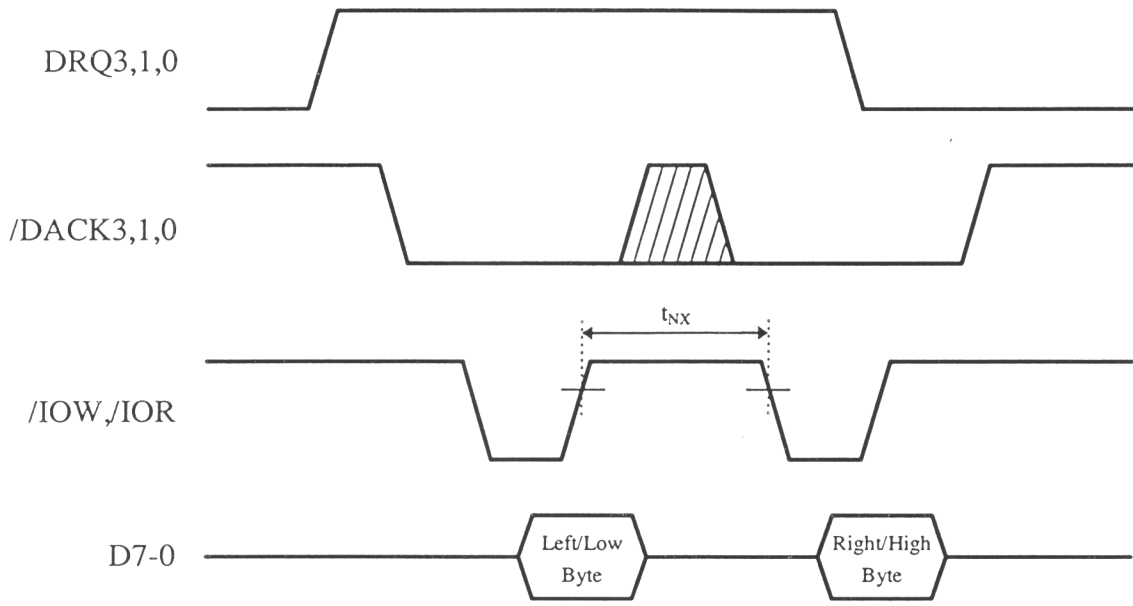


Fig.5

16bit Stereo DMA Cycle

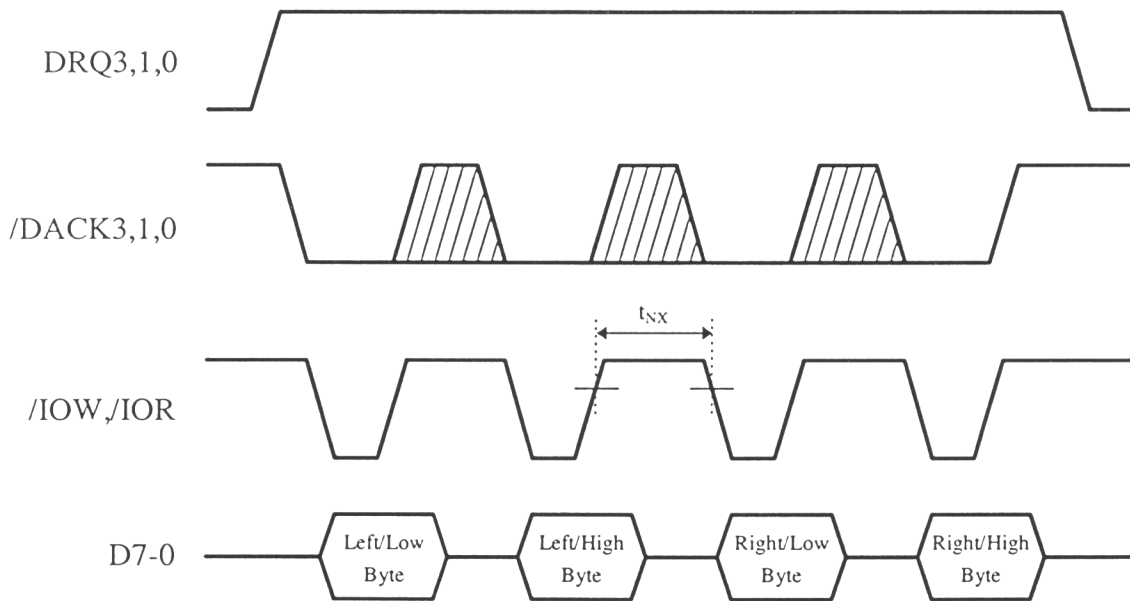


Fig.6

External Interface (External Synthesizer, CD ROM, Modem)

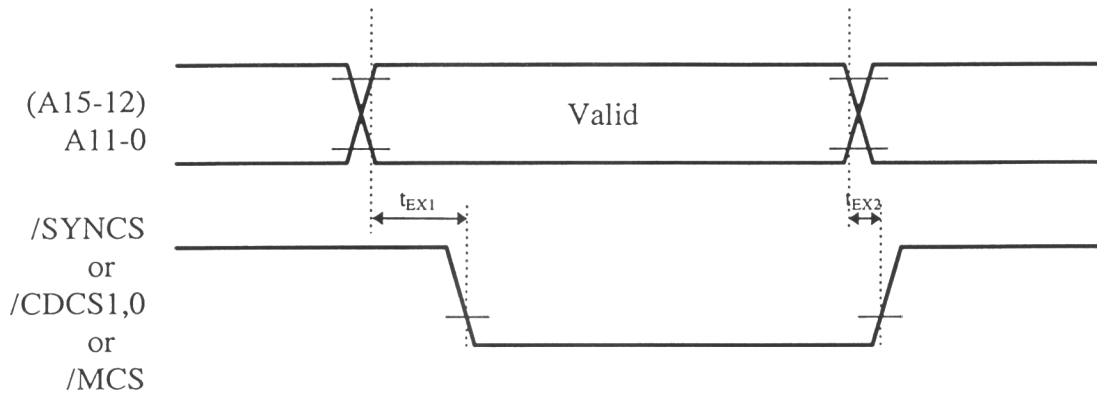


Fig.7

Reset Pulse Width

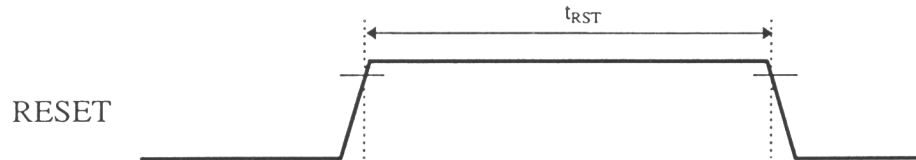


Fig.8

Serial Audio Interface

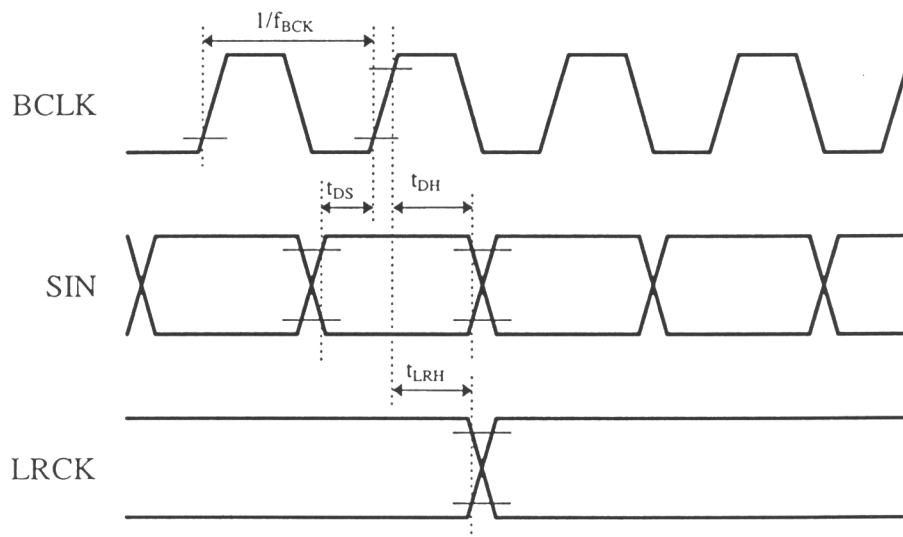


Fig.9

Analog Characteristics

Analog Input Characteristics

Item	Condition	Min.	Typ.	Max.	Unit
Full Scale V _{Input} · LINE/AUX1,2/MIN/MIC · MIC	+20dB	2.5	2.8	3.1	V _{pp}
		0.25	0.28	0.31	V _{pp}
ADC Resolution		16			bit
Recording Path(ADC) Dynamic Range · LINE/AUX1,2/MIN/MIC · MIC Distortion	+20dB		80		dB
			75		dB
			0.05		%
Interchannel Isolation		70			dB
L/R Channel Separation		70			dB
Gain Mismatch	from Spec.			0.5	dB
Frequency Response	20 to 15kHz	-3.0		0.5	dB
Input Resistance		20		100	k Ω
Input Capacitance				15	pF

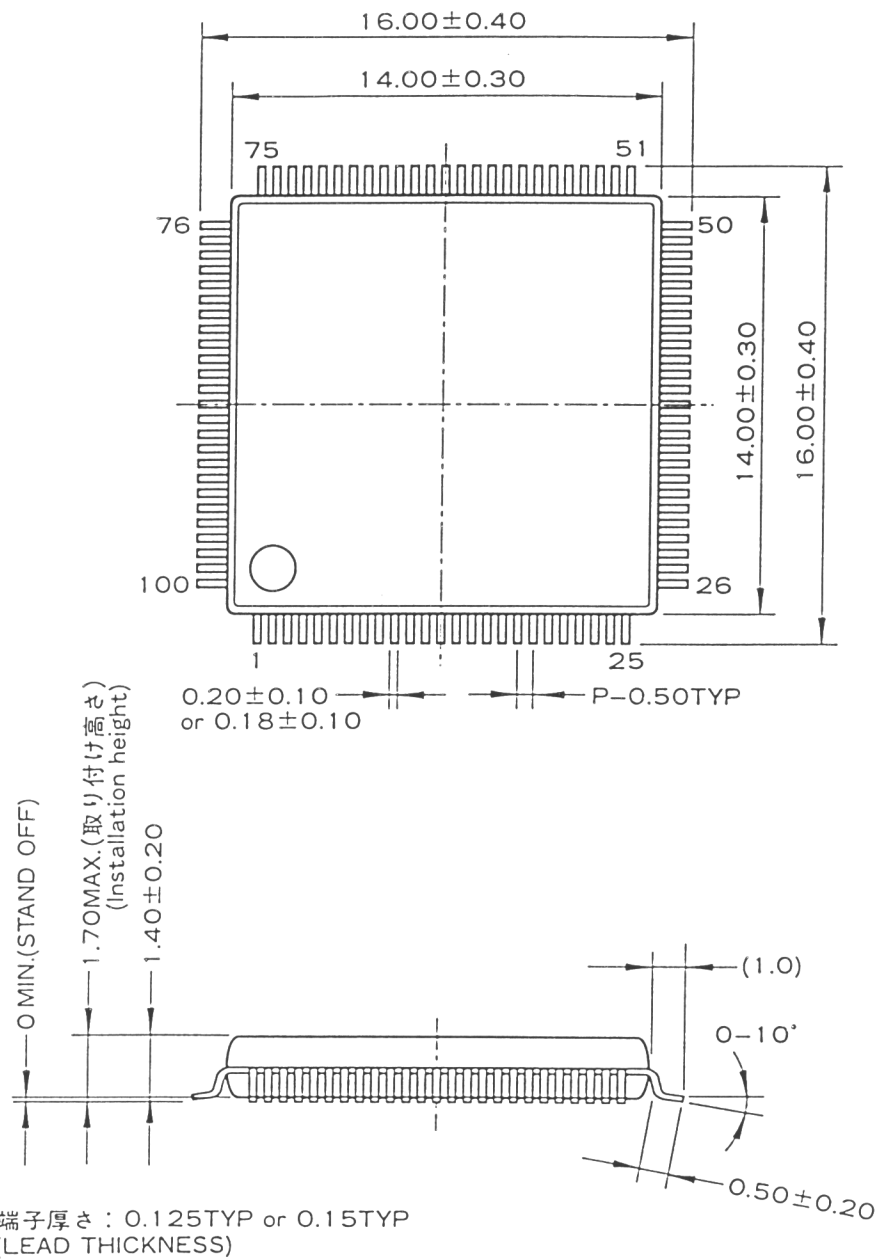
Note: DV_{SS}=AV_{SS}=0[V], T_{OP}=25°C, DV_{DD}=AV_{DD}=5.0[V]

Analog Output Characteristics

Item	Condition	Min.	Typ.	Max.	Unit
Full Scale Line Output · OLB=1 · OLB=0		2.4	2.8	3.1	V _{pp}
		1.7	2.0	2.2	V _{pp}
DAC Resolution · WSS_DAC · SB_DAC · FM_DAC		16			bit
		8			bit
		16			bit
Frequency Response · WSS_DAC · SB_DAC · FM_DAC	10 to 17.4 kHz	-0.5		0.5	dB
	10 to 15 kHz	-3.0		0.5	dB
	10 to 15 kHz	-3.0		0.5	dB
Mix_path Total Dynamic Range · from Input · from WSS_DAC · from SB_DAC Distortion · from Input · from WSS_DAC · from SB_DAC			85		dB
			80		dB
			50		dB
			0.01		%
			0.05		%
			0.30		%
FM Floating DAC · Dynamic Range · Distortion			85		dB
			0.30		%
Interchannel Isolation		70			dB
L/R Channel Separation		70			dB
Gain Mismatch	from Spec.			0.5	dB
Mute Attenuation		-80			dB
VREFO Voltage output		2.3	2.5	2.7	V

Note: DV_{SS}=AV_{SS}=0[V], T_{OP}=25°C, DV_{DD}=AV_{DD}=5.0[V]

External Dimensions



The shape of the molded corner may slightly differ from the shape in this diagram.

The figure in the parenthesis () should be used as a reference.

Plastic body dimensions do not include burr of resin.

UNIT: mm

Note : The LSIs for surface mount need especial consideration on storage and soldering conditions.

For detailed information, please contact your nearest agent of yamaha.

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_____ AGENCY _____

————— YAMAHA CORPORATION —————

Address inquires to :

Semi-conductor Sales Department

- **Head Office** 203, Matsunokijima, Toyooka-mura.
Iwata-gun, Shizuoka-ken. 438-01
Tel. 0539-62-4918 Fax. 0539-62-5054
- **Tokyo Office** 2-17-11, Takanawa, Minato-ku, Tokyo, 108
Tel. 03-5488-5431 Fax. 03-5488-5088
- **Osaka Office** 3-12-9, Minami Senba, Chuo-ku, Osaka City.
Osaka, 542 Shinsaibashi Plaza Bldg. 4F
Tel. 06-252-7980 Fax. 06-252-5615
- **U.S.A. Office** YAMAHA System Technology.
100 Century Center Court, San Jose, CA 95112
Tel. 408-467-2300 Fax. 408-437-8791

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